

# Compal confidential

## *LC-Marseille 10AD*

### PWWAE LA-6843P Schematics Document

Mobile AMD S1G4/ RS880M / SB820M

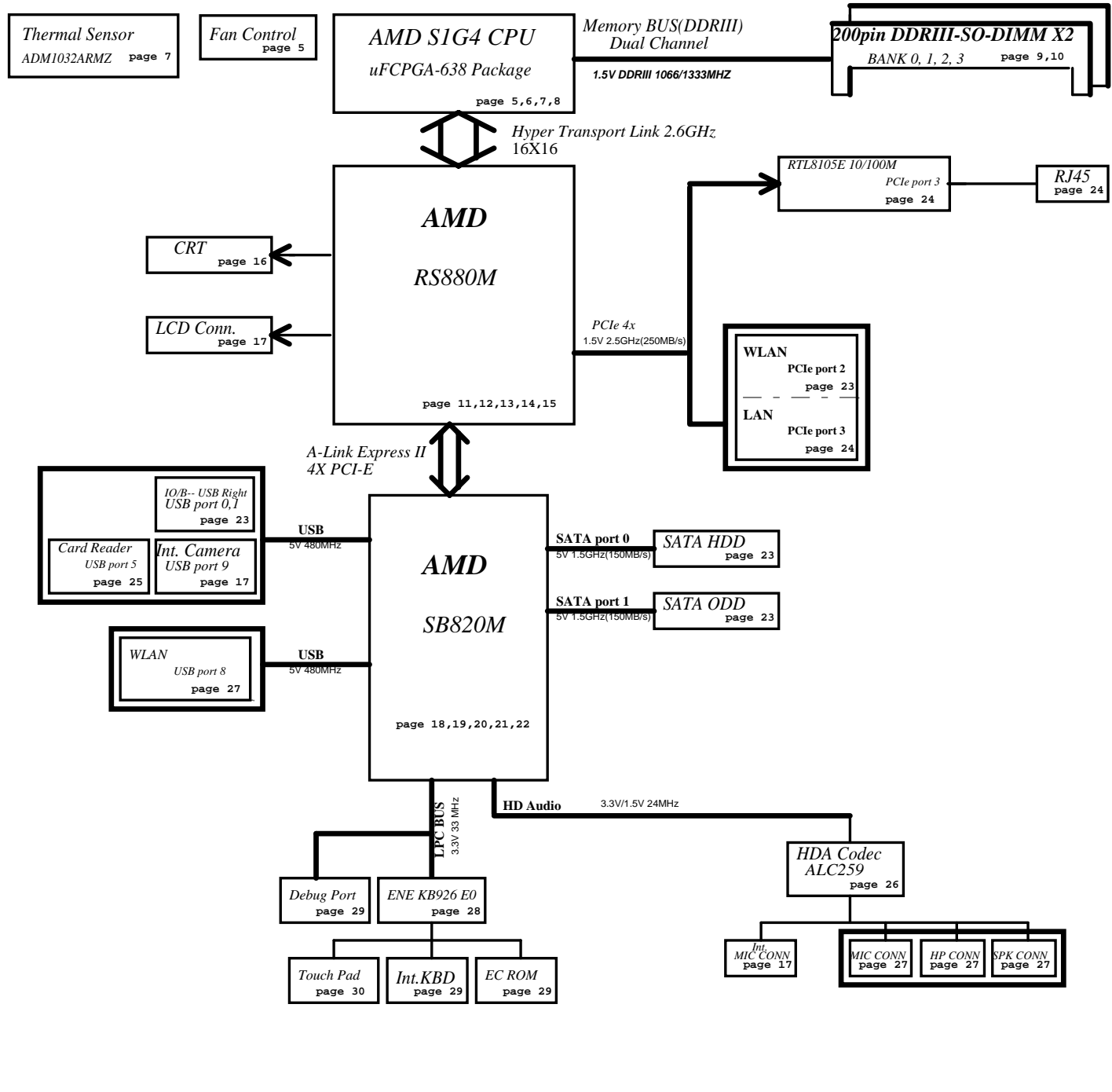
2010-08-16 Rev. 1.0

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# Compal Confidential

Model Name : PWWAA

File Name : LA-6843P



RTC CKT.

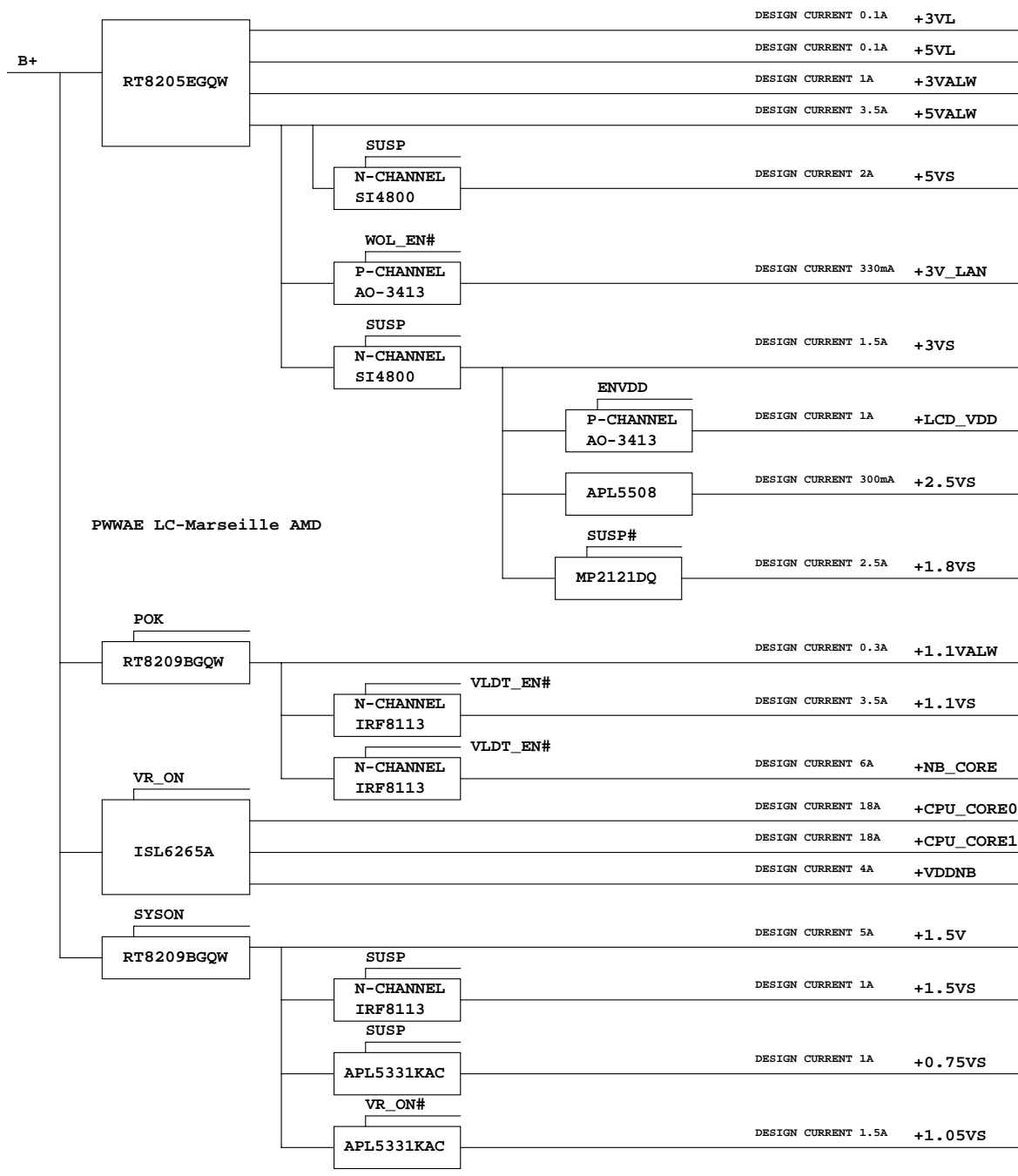
Power On/Off CKT.  
page 30

DC/DC Interface CKT.  
page 31

Power Circuit DC/DC  
page 31, 32, 33, 34, 35  
36, 37, 38, 39

Power/B  
page 30

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PWWAE LC-Marseille AMD

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### Voltage Rails

O : ON  
X : OFF

State	+B +3VL +5VL +RTCVC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +1.05VS +0.75VS +VGA_CORE +VDDNB +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Platform	CPU	NB	VGA	SB	Comment
Danube	S1G4	RS880M	NA	SB820M	

@ : just reserve , no build  
**SB820MR1@** : just reserve for SB820MR1 only  
**R3@** : just reserve for R3 only  
**CONN@** : just reserve for Connector only  
**CAM@** : just reserve for WebCam only  
**BT@** : just reserve for Blue Tooth only  
**880MR1@** : just reserve for 880MR1 only  
**8105E\_VC@** : just reserve for 10/100 LAN VC version only  
**8105E\_VB@** : just reserve for 10/100 LAN VBversion only

### BTO (Build-To-Order) Option Table

Function	Camera					
Description	( C )					
Explain						
BTO	CAM@					

### I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 0

### EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001 011X b
EC KB926E0		

### EC SM Bus2 address

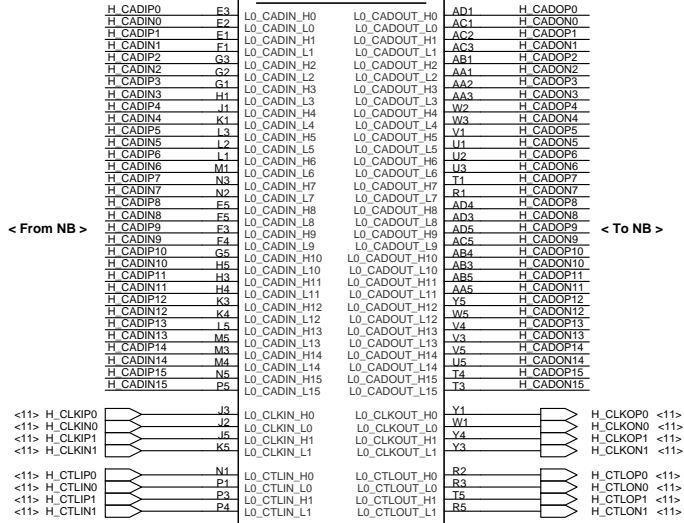
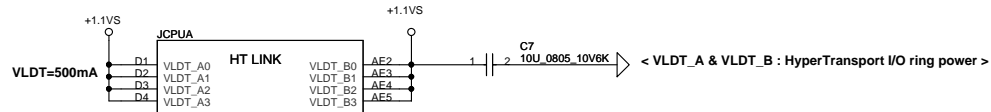
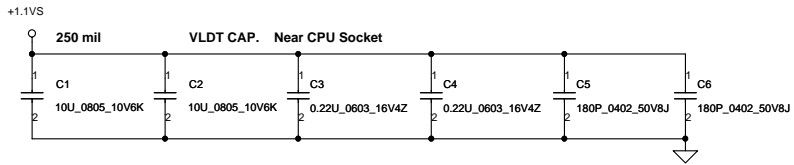
Device	HEX	Address
EMC1032-1 CPU 98H		1001 100X b
EC KB926E0		

### SMBUS Control Table

	SOURCE	BATT	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM
EC_SMB_CK1 EC_SMB_DA1	KB926	V					
EC_SMB_CK2 EC_SMB_DA2	KB926		V				
I2C_CLK I2C_DATA	RS880M						V
DDC_CLK0 DDC_DATA0	RS880M						
SCL0 SDA0	SB820			V	V		
SCL1 SDA1	SB820					V	

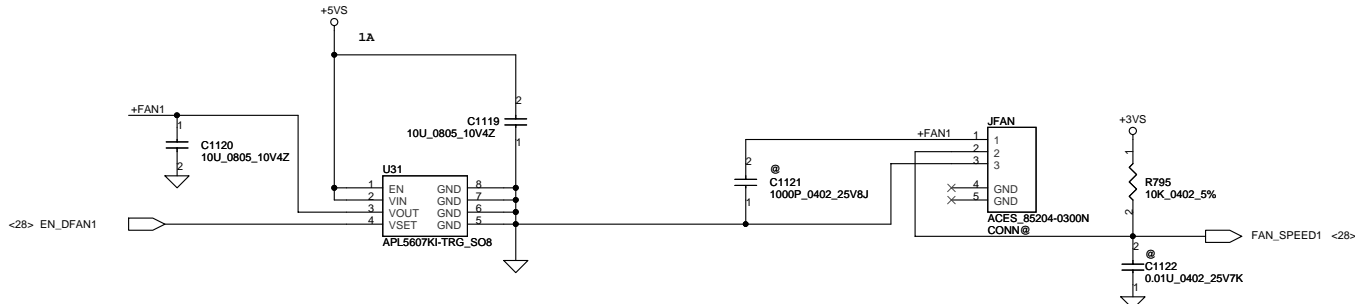
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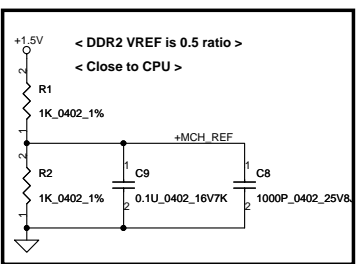


FOX\_PZ6382A-284S-41F\_Champian  
CONN@

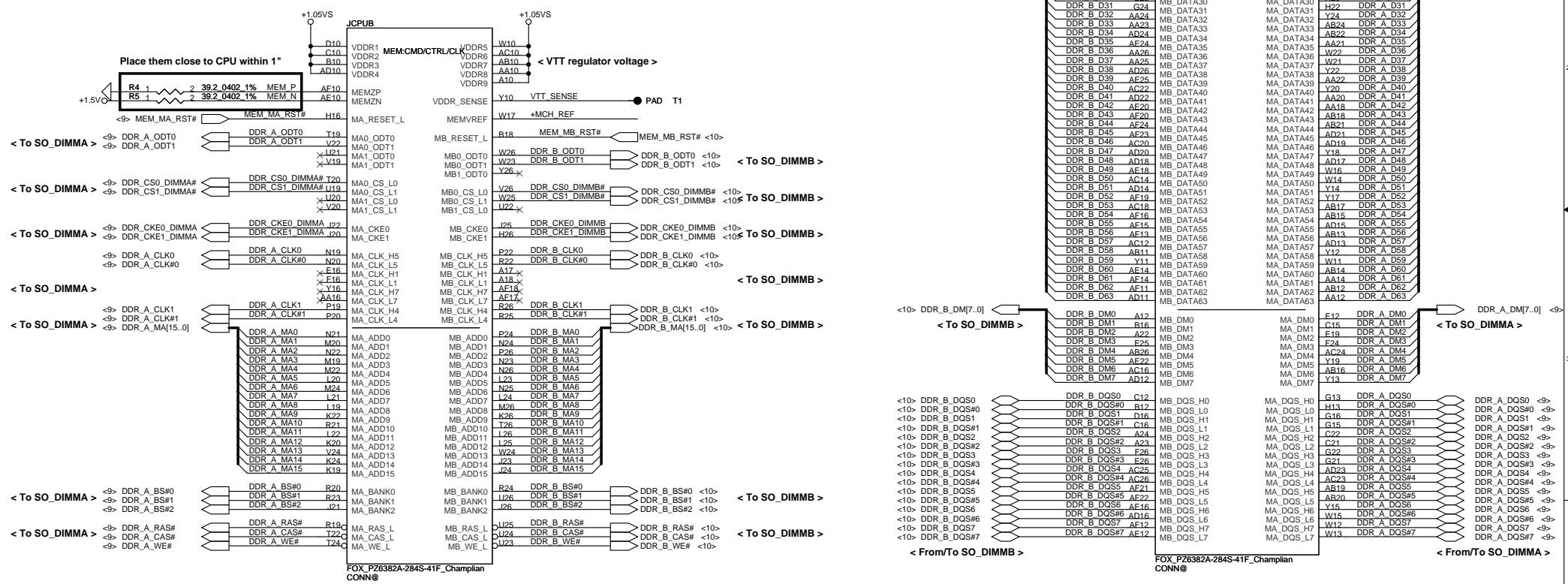
< FAN Control Circuit :  $V_{out} = 1.6 \times V_{set}$  >



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< Processor DDR3 Memory Interface >



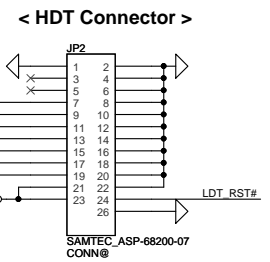
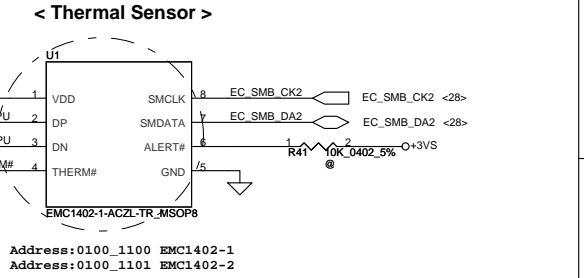
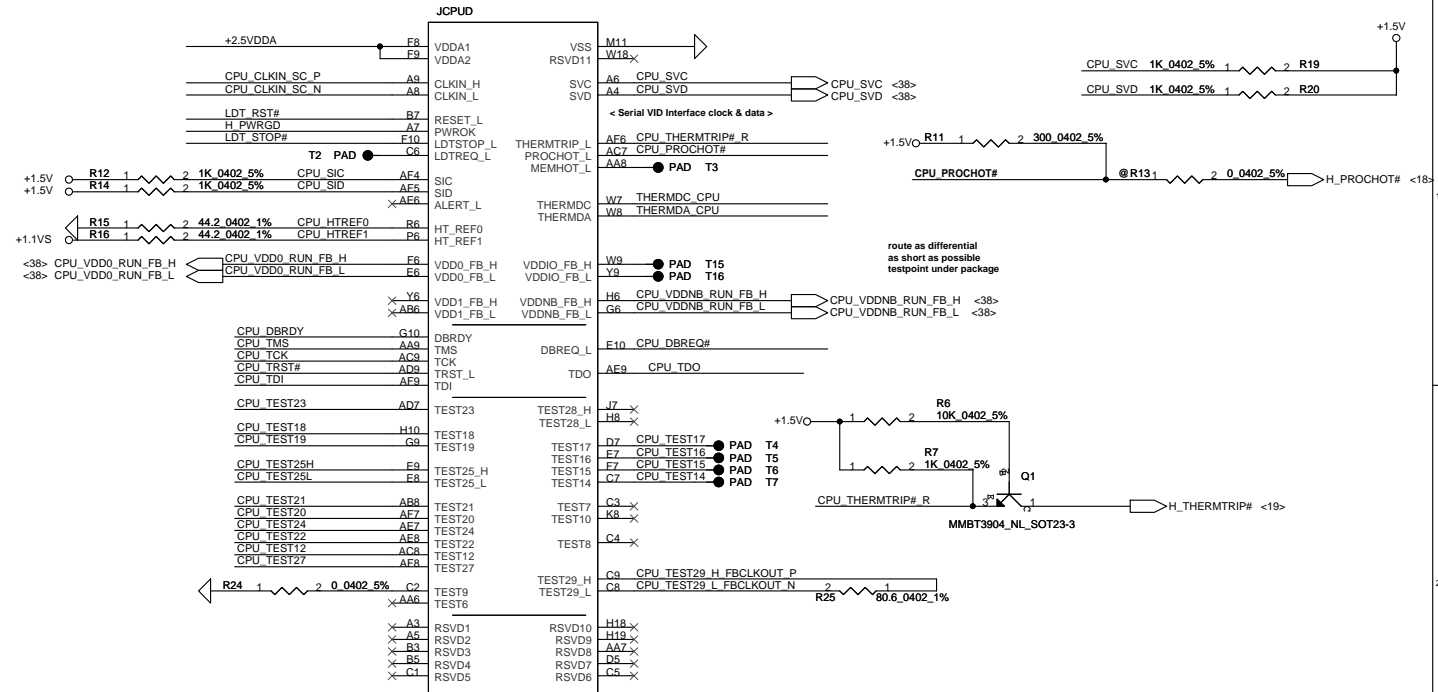
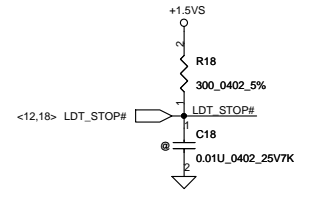
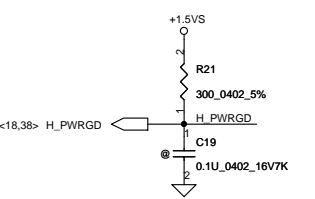
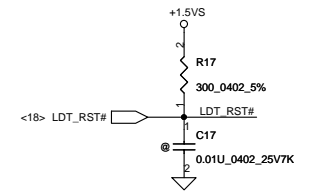
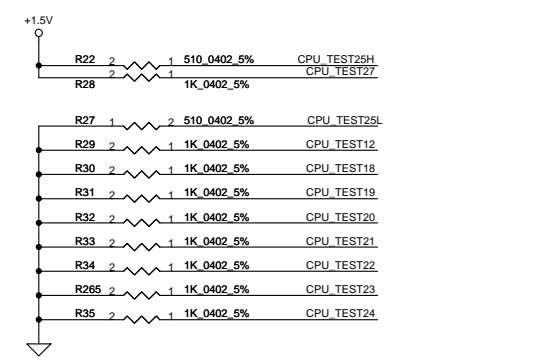
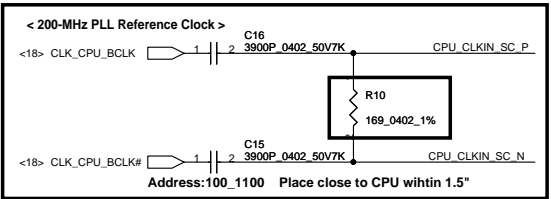
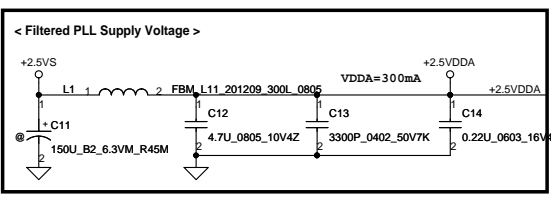
FOX\_PZ6382A-284S-41F\_Champlain CONN@

FOX\_PZ6382A-284S-41F\_Champlain CONN@

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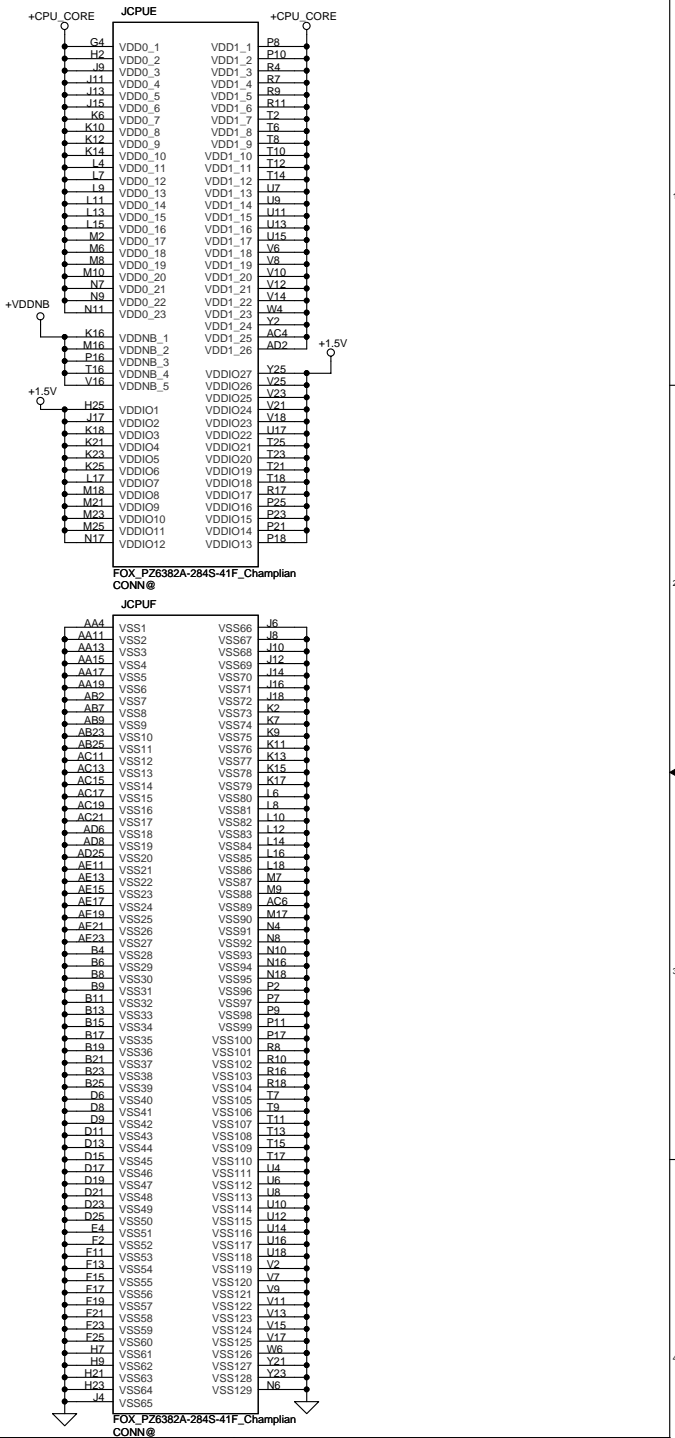
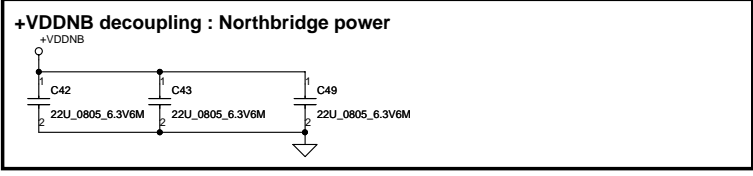
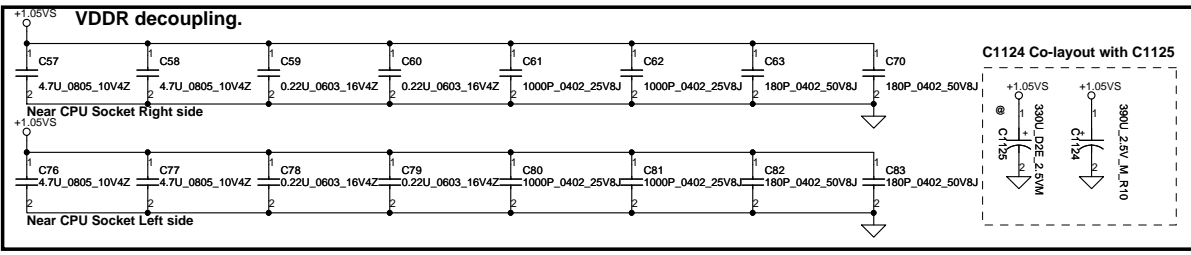
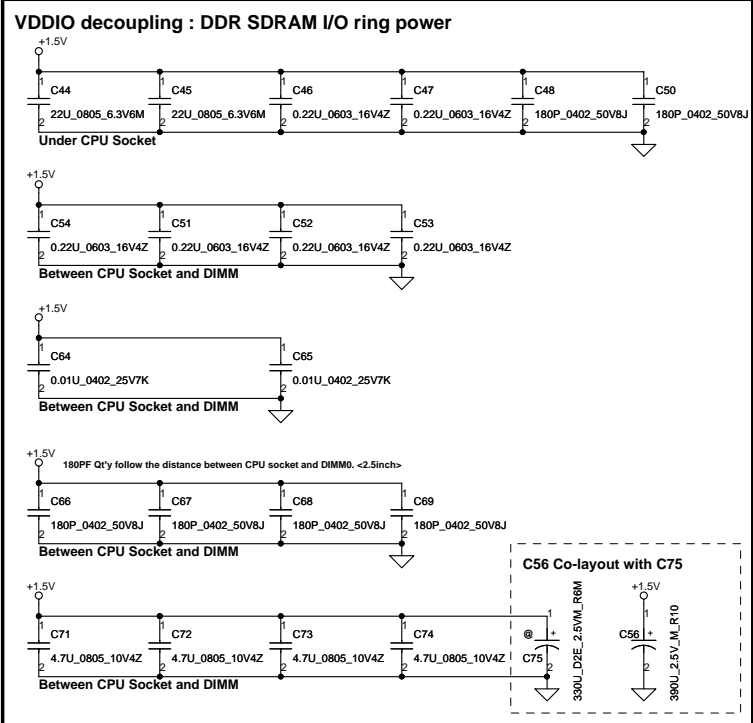
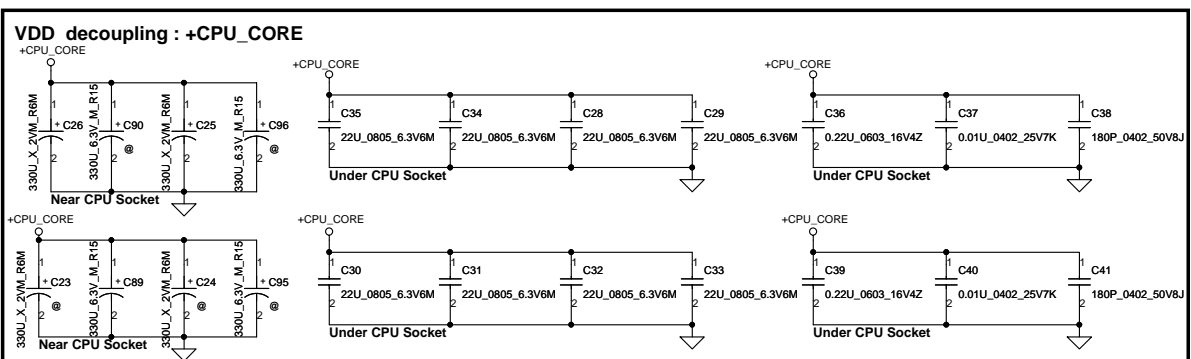
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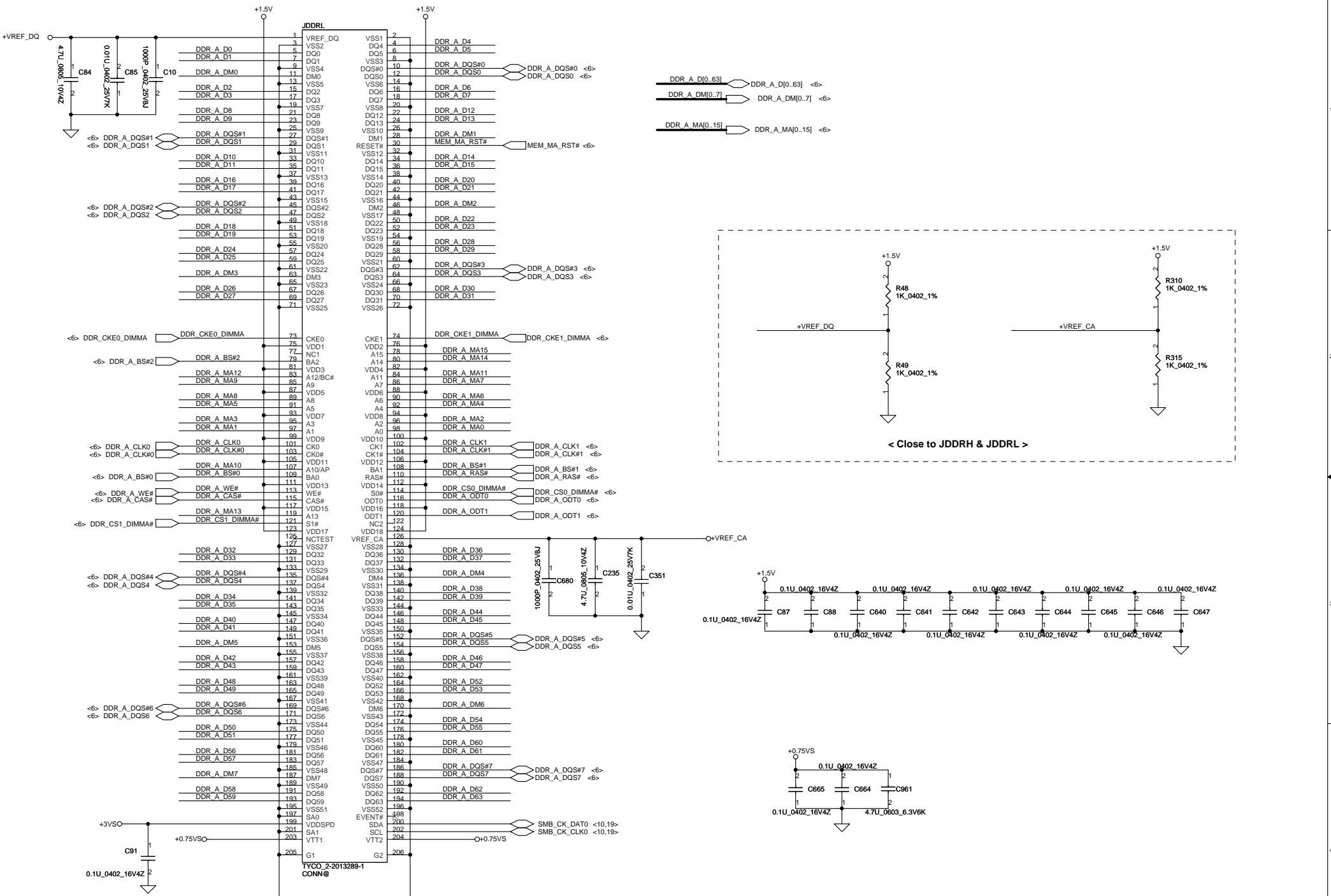
3/30 Change U1 ADM1032 to EMC1402 for cost down

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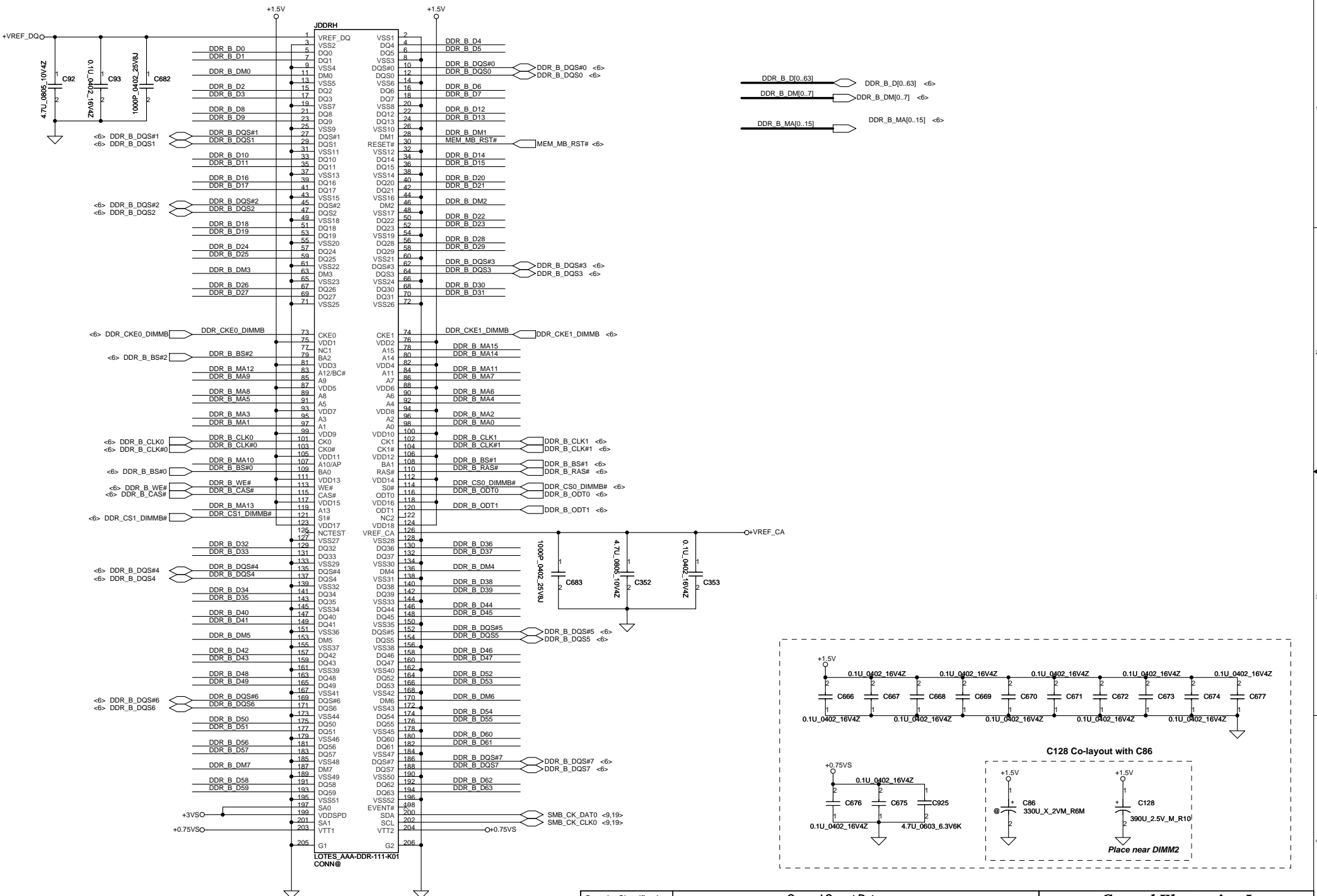
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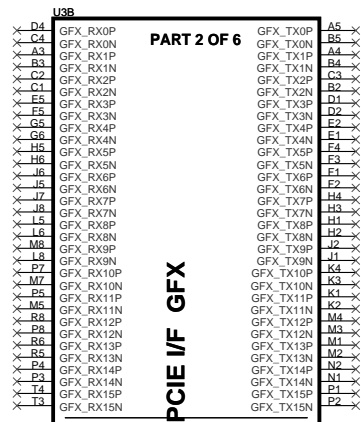
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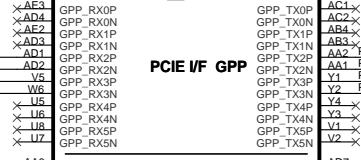


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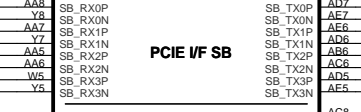
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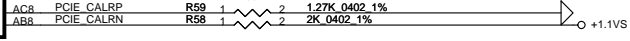
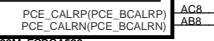
**PCIE I/F GFX**



**PCIE I/F GPP**



**PCIE I/F SB**



**PCIE PORT LIST**

PORT	DEVICE
PCIE-2	WLAN
PCIE-3	LAN

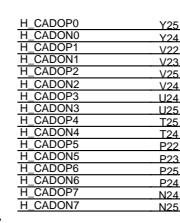
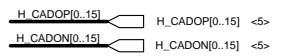
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< LAN >

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< From SB820 : x4 PCIE A-link >

< To SB820 : x4 PCIE A-link >

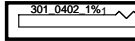
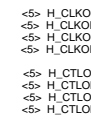
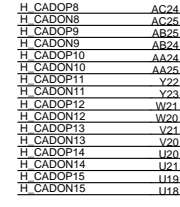
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**HYPER TRANSPORT CPU I/F**

< To S1G4 CPU : x16 HT >

< From S1G4 CPU : x16 HT >

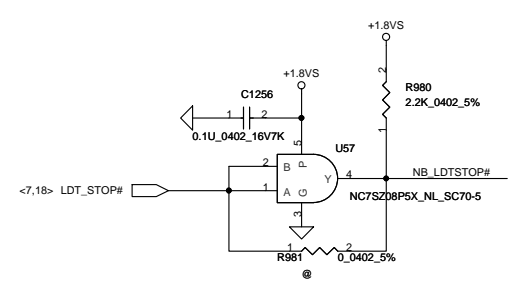
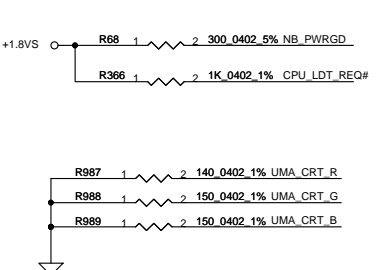
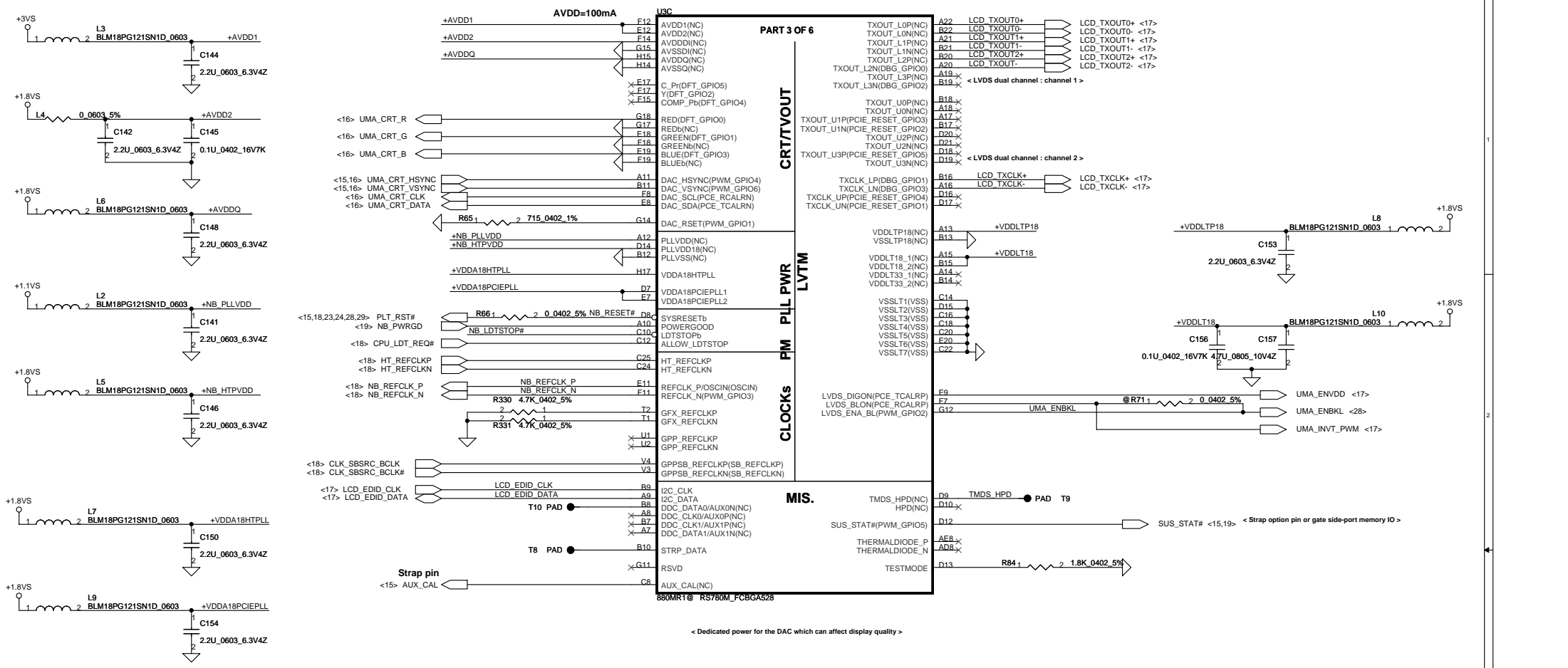


0718 Place within 1" layout 1:2

0718 Place within 1" layout 1:2

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U3D

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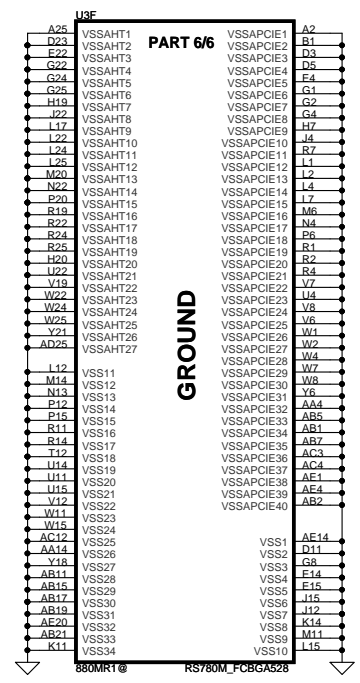
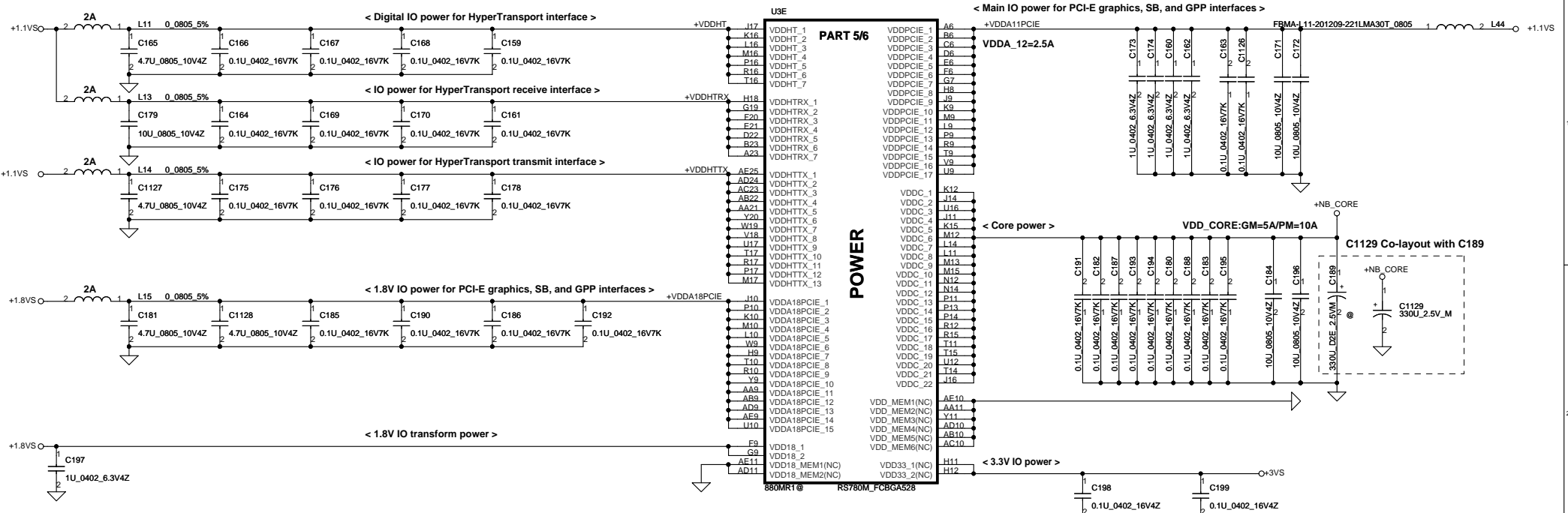
AB12	MEM_A0(NC)	MEM_DQ0/DVO_VSYNC(NC)	AA18
AE16	MEM_A1(NC)	MEM_DQ1/DVO_HSYNC(NC)	AA20
Y11	MEM_A2(NC)	MEM_DQ2/DVO_DE(NC)	AA15
AE15	MEM_A3(NC)	MEM_DQ3/DVO_D0(NC)	Y19
AA12	MEM_A4(NC)	MEM_DQ4(NC)	V17
AB16	MEM_A5(NC)	MEM_DQ5/DVO_D1(NC)	AA17
AB14	MEM_A6(NC)	MEM_DQ6/DVO_D2(NC)	AA15
AD14	MEM_A7(NC)	MEM_DQ7/DVO_D4(NC)	Y15
AD13	MEM_A8(NC)	MEM_DQ8/DVO_D3(NC)	AC20
AD15	MEM_A9(NC)	MEM_DQ9/DVO_D5(NC)	AD19
AC16	MEM_A10(NC)	MEM_DQ10/DVO_D6(NC)	AE22
AE13	MEM_A11(NC)	MEM_DQ11/DVO_D7(NC)	AC18
AC14	MEM_A12(NC)	MEM_DQ12/DVO_D8(NC)	AB20
Y14	MEM_A13(NC)	MEM_DQ13/DVO_D9(NC)	AD22
AD16	MEM_BA0(NC)	MEM_DQ14/DVO_D10(NC)	AC22
AE17	MEM_BA1(NC)	MEM_DQ15/DVO_D11(NC)	AD21
AD17	MEM_BA2(NC)		
W12	MEM_RASb(NC)	MEM_DQS0/DVO_IDCKP(NC)	Y17
Y12	MEM_CASb(NC)	MEM_DQS0/DVO_IDCKN(NC)	W18
AD18	MEM_WEB(NC)	MEM_DQS1(NC)	AD20
AB13	MEM_CSB(NC)	MEM_DQS1(NC)	AE21
AB18	MEM_CKE(NC)	MEM_DM0(NC)	W17
Y14	MEM_ODT(NC)	MEM_DM1/DVO_D8(NC)	AE19
V15	MEM_CKPN(NC)	IOPLLVD18(NC)	AE23
W14	MEM_CKN(NC)	IOPLLVD18(NC)	AE24
AE12	MEM_COMPN(NC)	IOPLLVS(NC)	AD23
AD12	MEM_COMPN(NC)	MEM_VREF(NC)	AE18

**SBD\_MEM/DVO\_I/F**

880MR1@

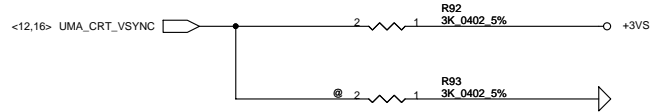
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< RS880 VSYNC mux at CRT\_VSYNC pull High to 3K >



< VSYNC : STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb >

Enables the Test Debug Bus using GPIO.

- 1 : Disable (RX881, RS880)
- 0 : Enable (RX881, RS880)

PIN: RS880--> VSYNC#

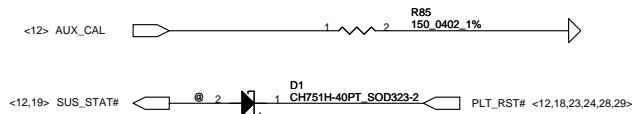
< RS880 use register to control PCI-E configure >

< DFT\_GPIO[4:2] : STRAP\_PCIE\_GPP\_CFG[2:0] >

These pin straps are used to configure PCI-E GPP mode.

- 000 : 00001
- 001 : 00010
- 010 : 01011
- 011 : 00100
- 100 : 01010
- 101 : 01100
- 111 : 01011

< RS880 SUS\_STAT# >



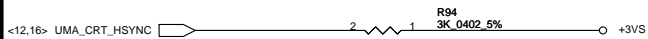
< SUS\_SATA# : LOAD\_EEPROM\_STRAPS >

Selects Loading of STRAPS from EPROM

- 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
- 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS880:SUS\_STAT#

< RS880 use HSYNC to enable SIDE PORT (internal pull high) >



< HSYNC : STRAP\_DEBUG\_BUS\_PCIE\_ENABLEb >

RX881: Enables the Test Debug Bus using PCIE bus

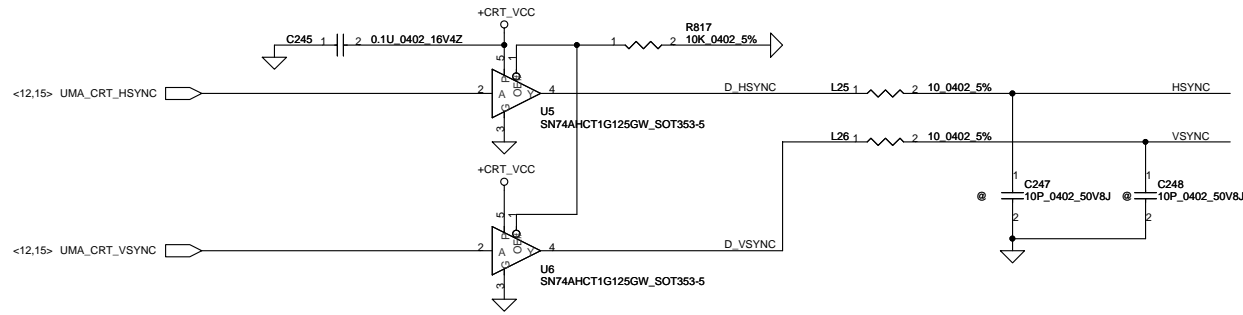
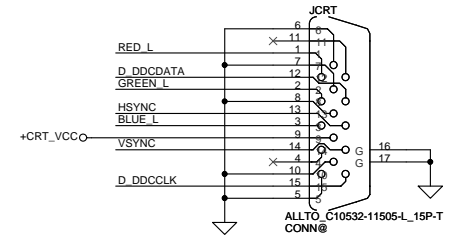
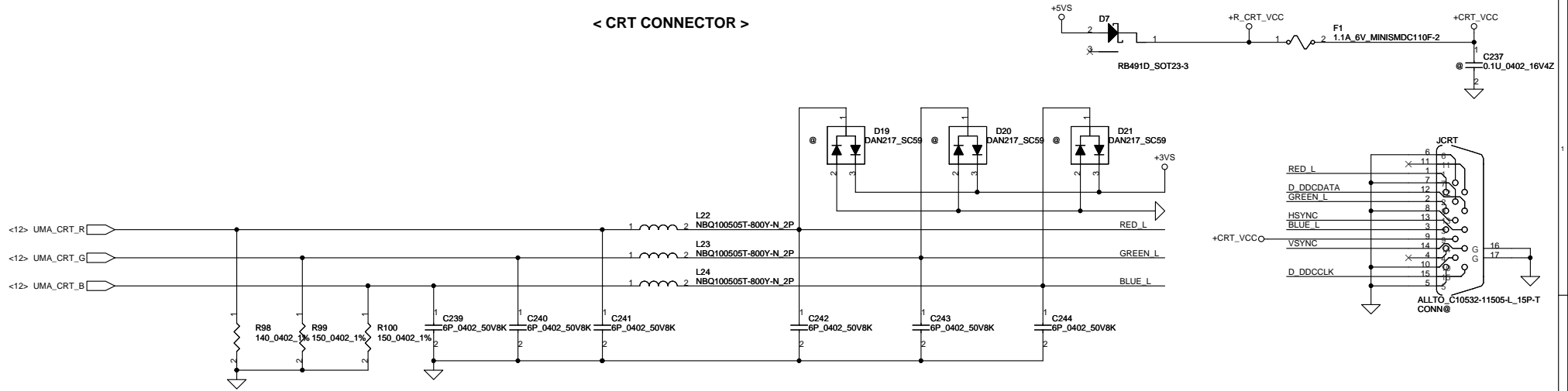
- 1 : Disable ( Can still be enabled using nbcfg register access )
- 0 : Enable

RS880: Enables Side port memory ( RS780 use HSYNC#)

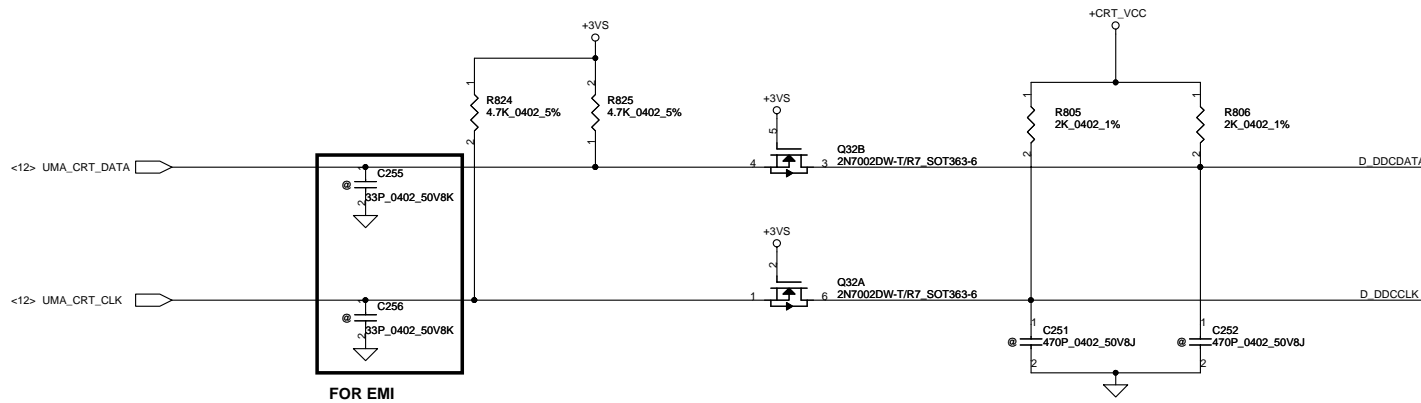
- 1. Disable (RS880)
- 0 : Enable (RS880)

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< CRT CONNECTOR >



< SYNC SIGNAL >



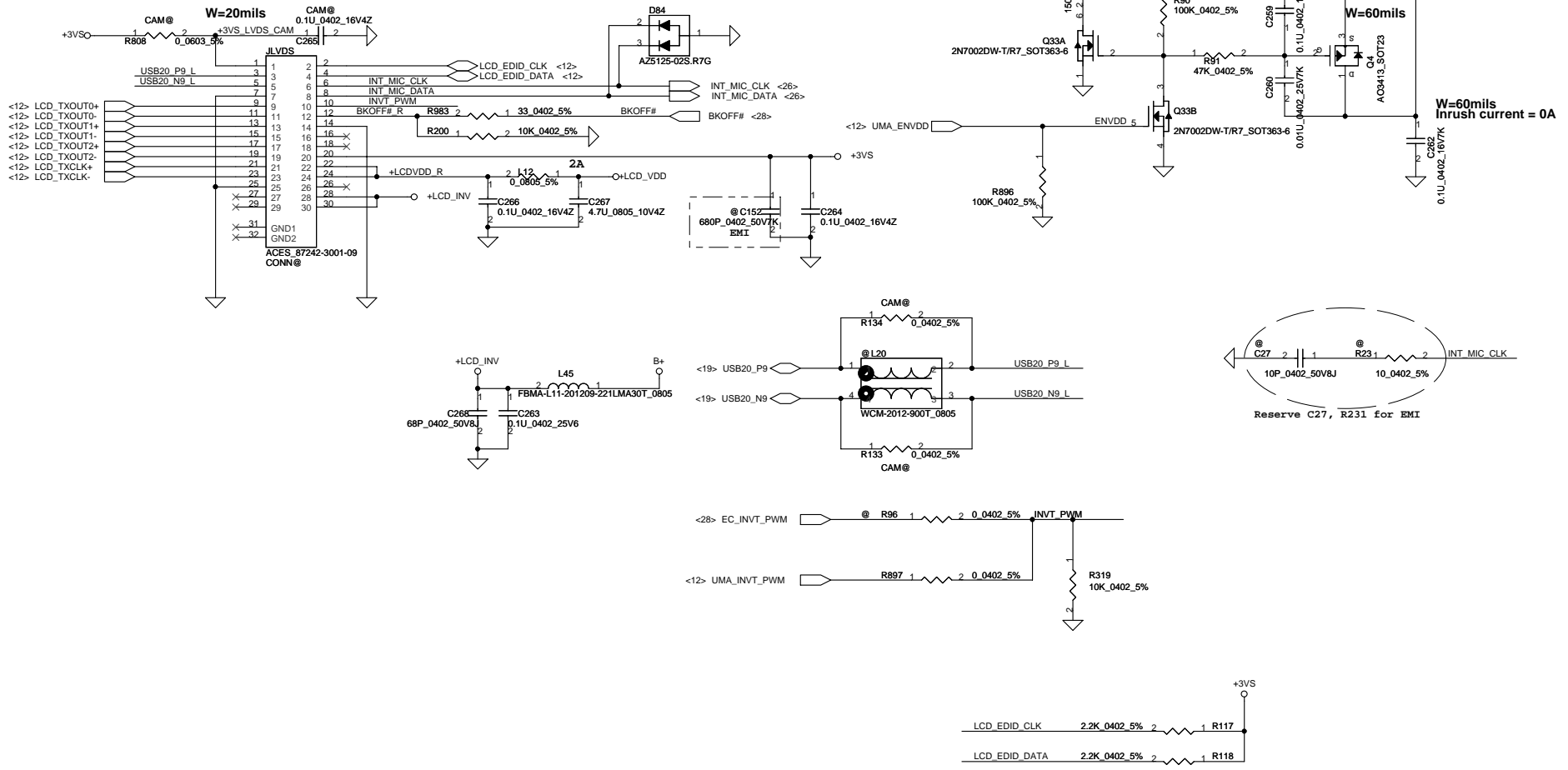
< Display Data Channel >

FOR EMI

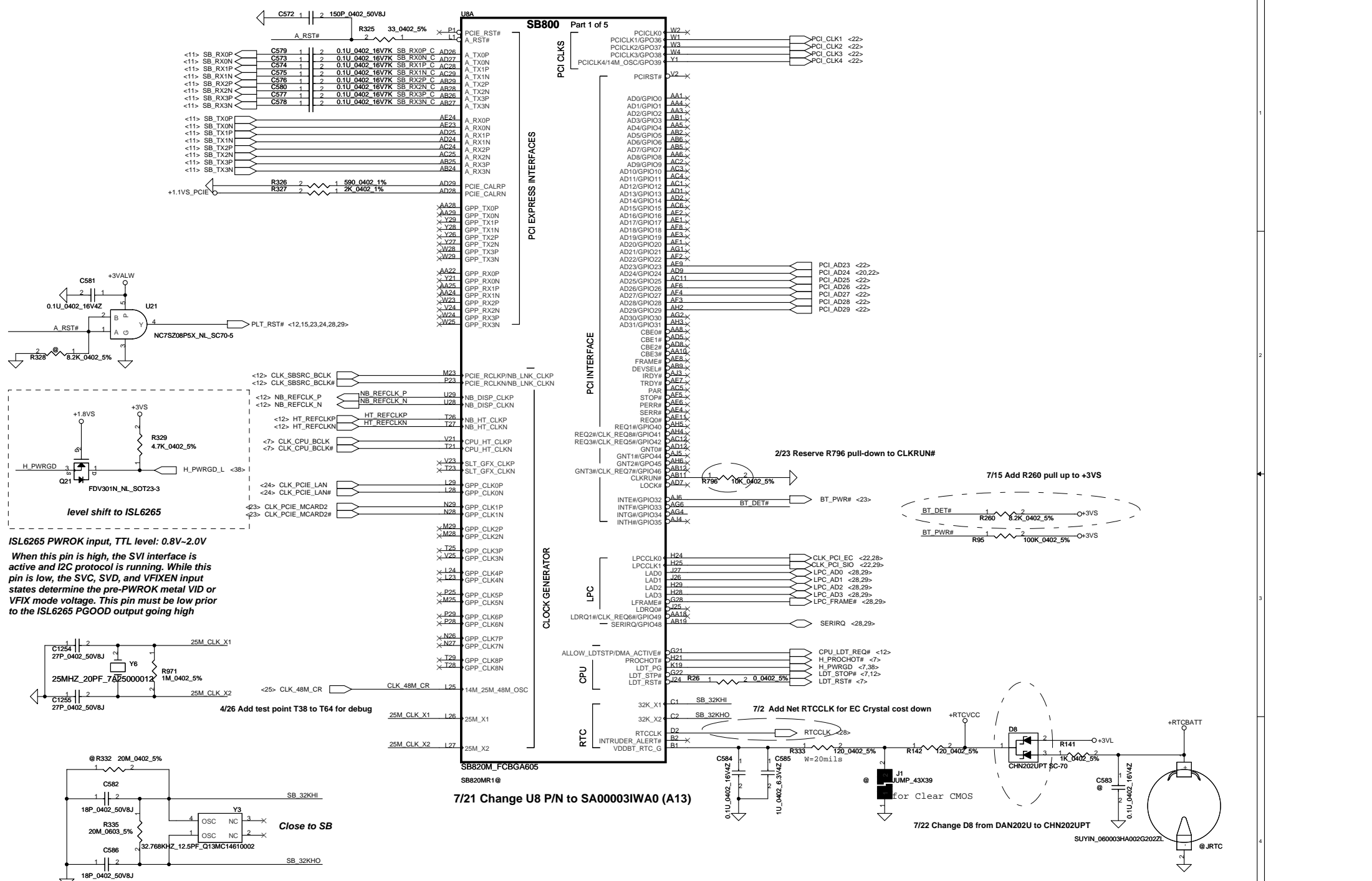
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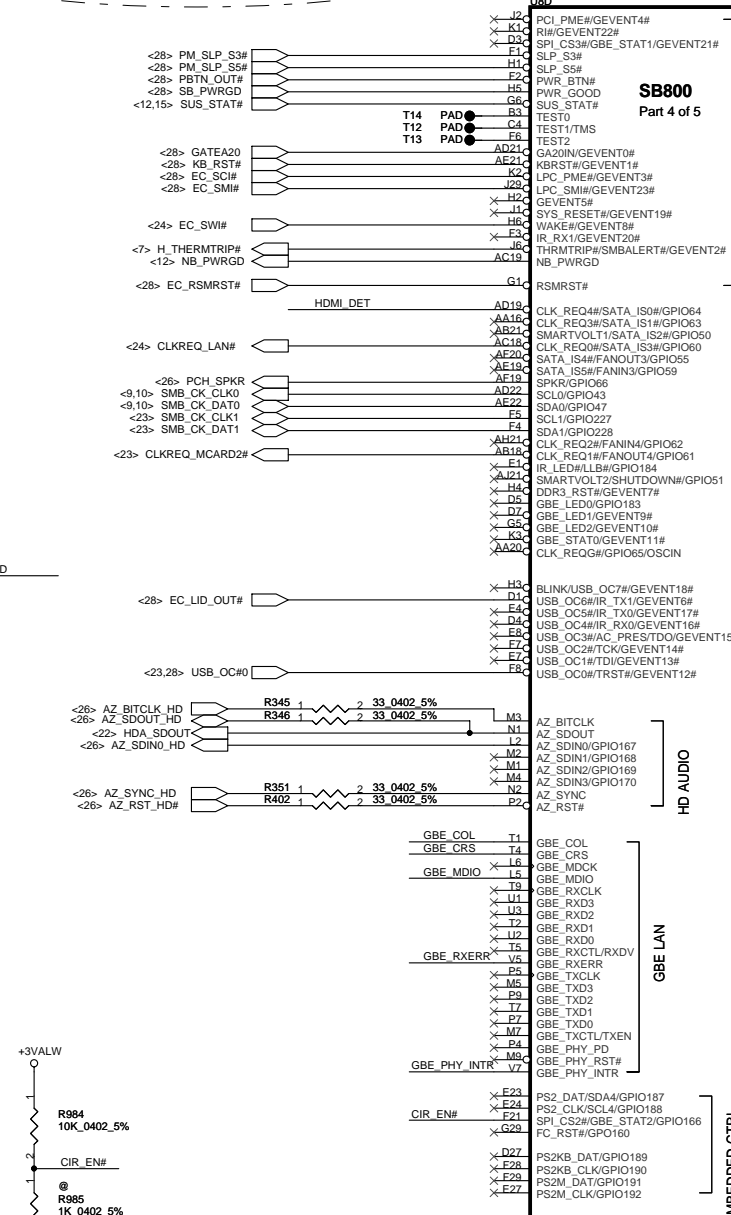
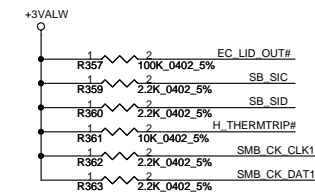
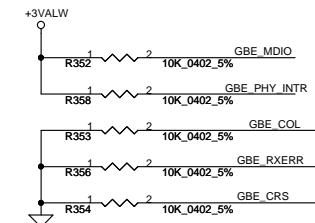
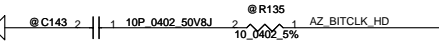
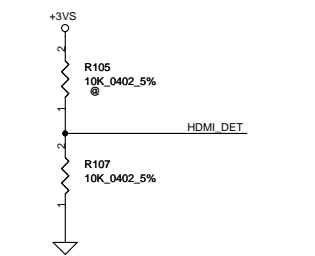
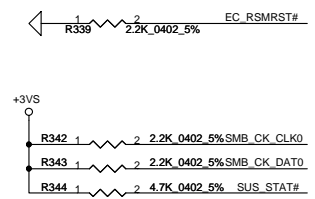
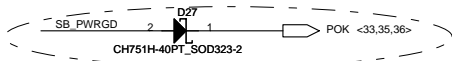
# LCD/PANEL BD. Conn.



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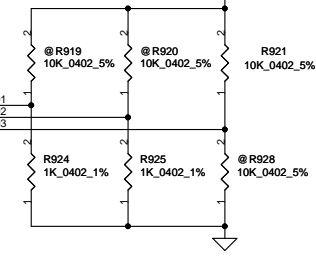
7/2 Add D27 for abnormal shutdown RSMRST#



SB800  
Part 4 of 5

PORT	DEVICE
USB0	USB0(Right)
USB1	USB1(Right)
USB5	Card Reader
USB8	WLAN
USB9	Int Camera

STRAP PIN



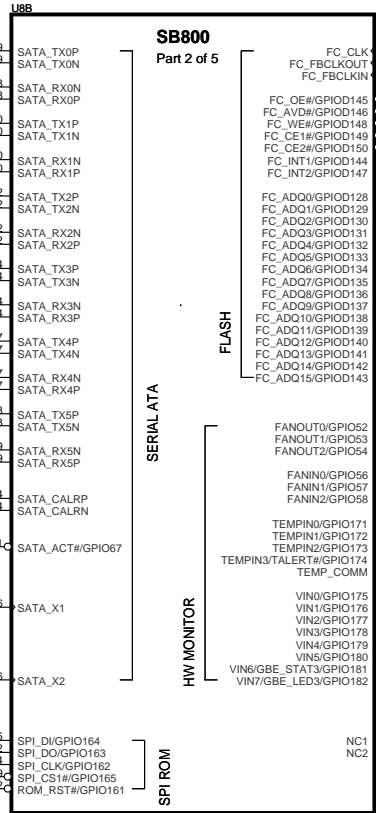
	GPIO204	GPIO205
Nile-M	High	High
Nile-S	High	High
Danube Marseille	Low	Low
Danube Hamburg	Low	High
None	Low	High
Park XT	High	Low
M92 XTX	High	High

HDD

<23> SATA\_STX\_DRX\_P0  
<23> SATA\_STX\_DRX\_N0

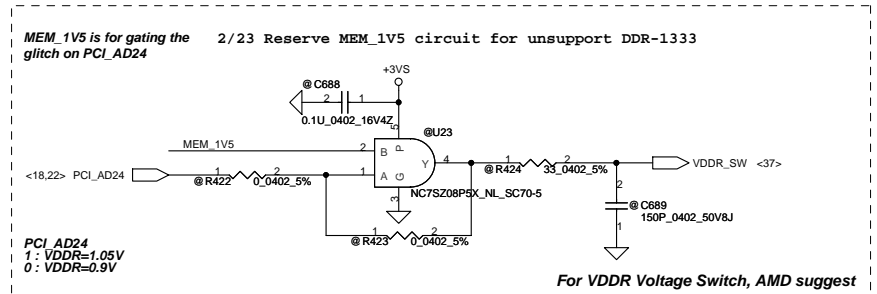
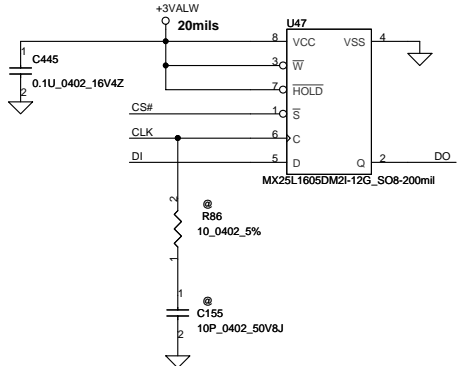
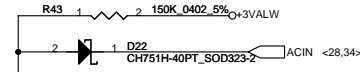
ODD

<23> SATA\_SRX\_C\_DTX\_N0  
<23> SATA\_SRX\_C\_DTX\_P0  
<23> SATA\_STX\_DRX\_P1  
<23> SATA\_STX\_DRX\_N1  
<23> SATA\_SRX\_C\_DTX\_N1  
<23> SATA\_SRX\_C\_DTX\_P1

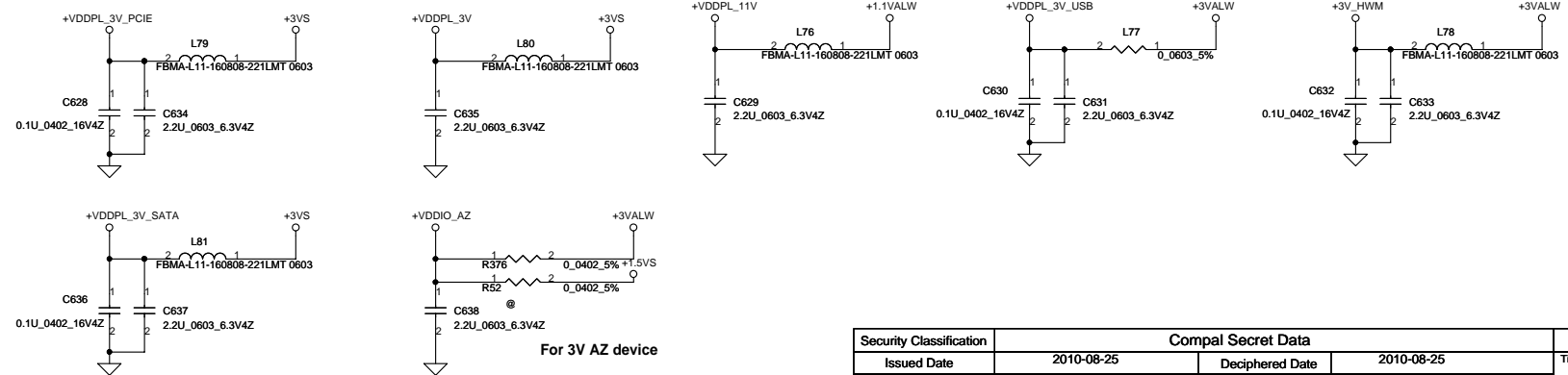
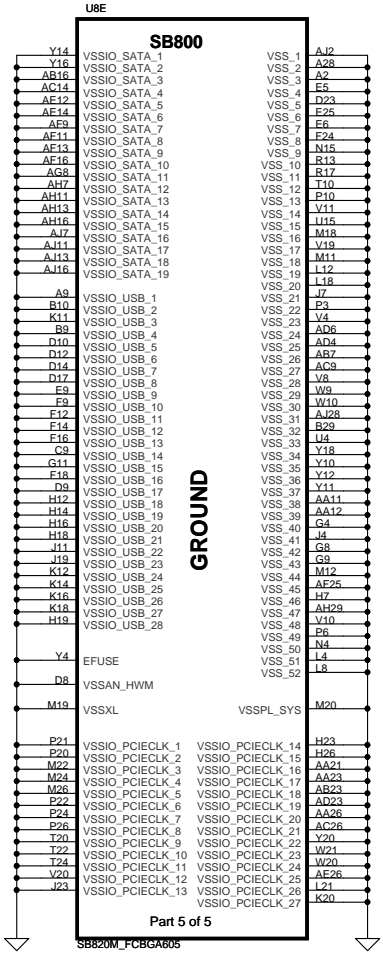
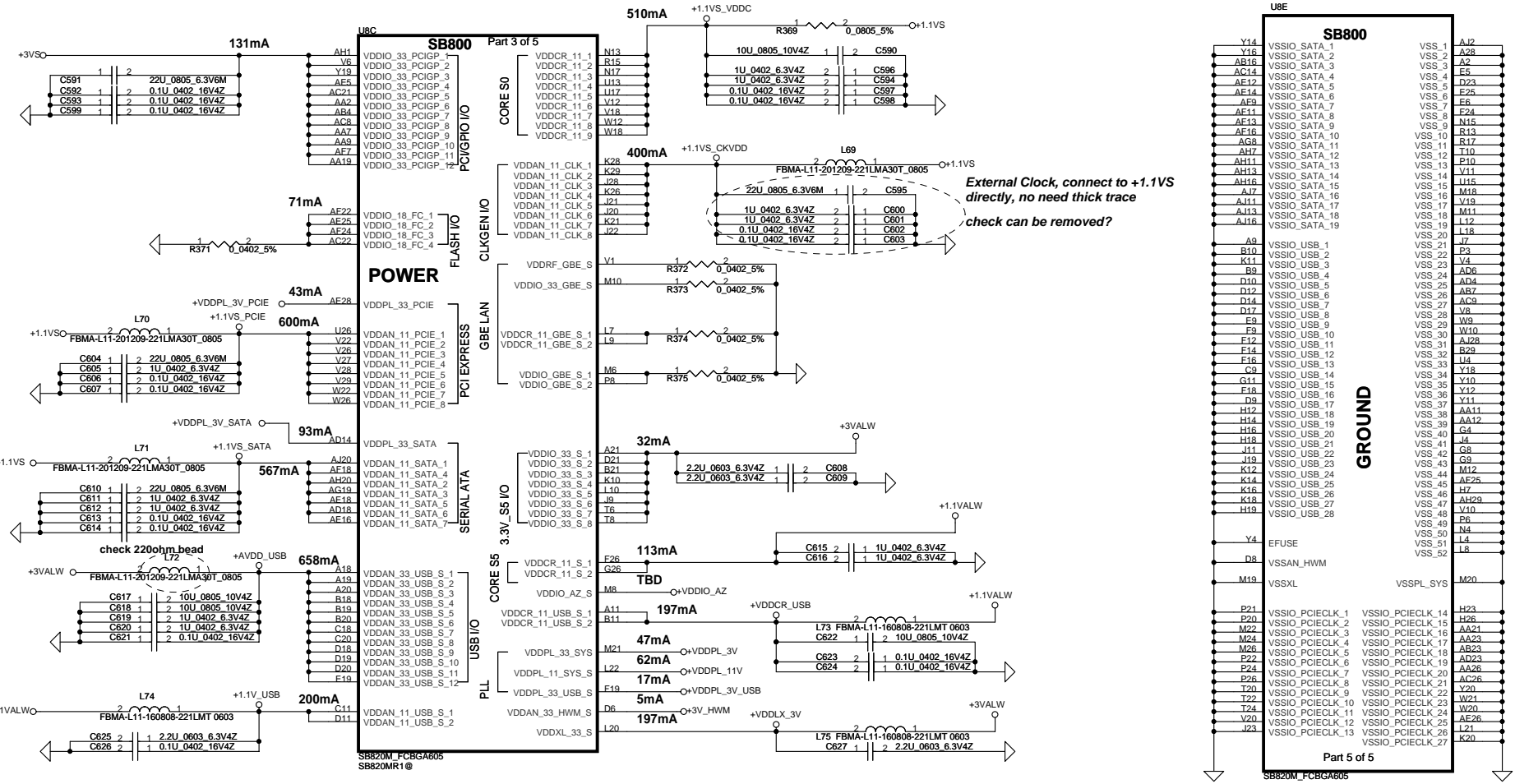


+1.1VS\_SATA

R364 2 1K 0402 1% SATA\_CALRP  
R365 2 931 0402 1% SATA\_CALRN



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For 3V AZ device

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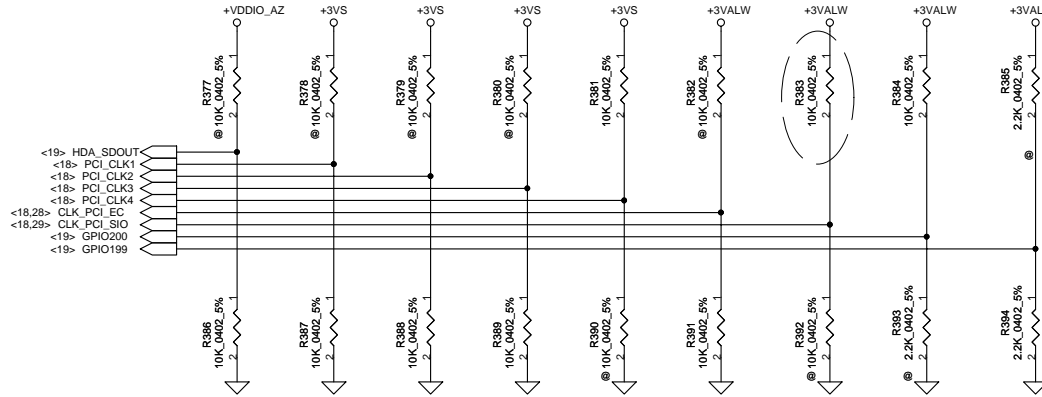
Compal Electronics, Inc.

SHEMATICS, MB A6843

# REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
<b>PULL HIGH</b>	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Enable DEFAULT	EC ENABLE	CLOCKGEN ENABLE DEFAULT	H,H = Reserved H,L = SPI ROM (Default)	
<b>PULL LOW</b>	Performance MODE DEFAULT	FORCE PCIE GEN1 DEFAULT	WATCHDOG TIMER DISABLE DEFAULT	IGNORE DEBUG STRAP DEFAULT	Inter CLK Gen Mode Disable	EC DISABLE DEFAULT	CLOCKGEN DISABLE	L,H = LPC ROM L,L = FWH ROM	



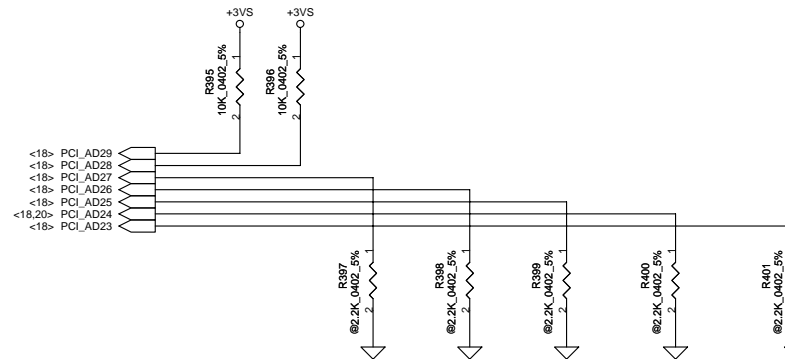
# DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

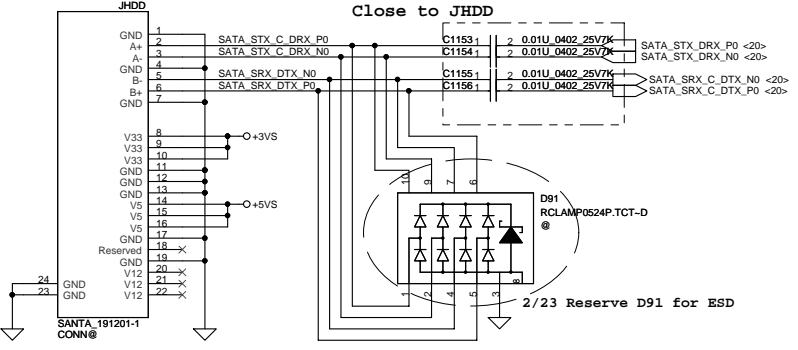
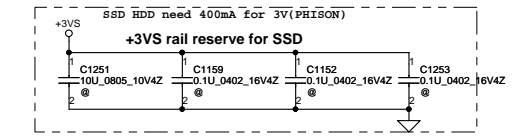
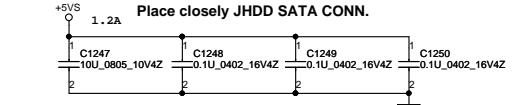
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Check AD29,AD28 strap function

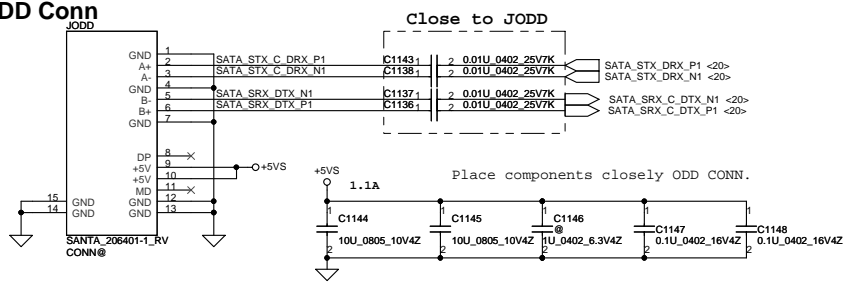
check default



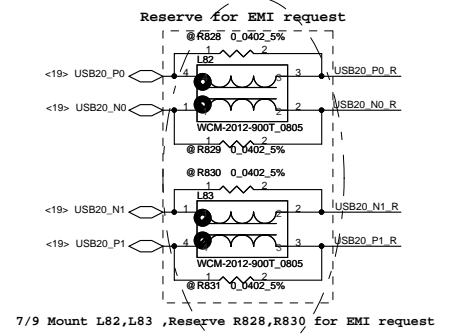
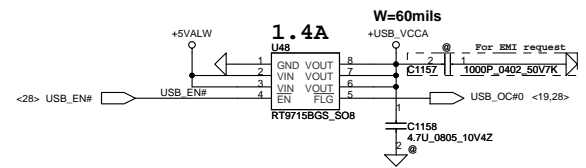
### SATA HDD Conn.



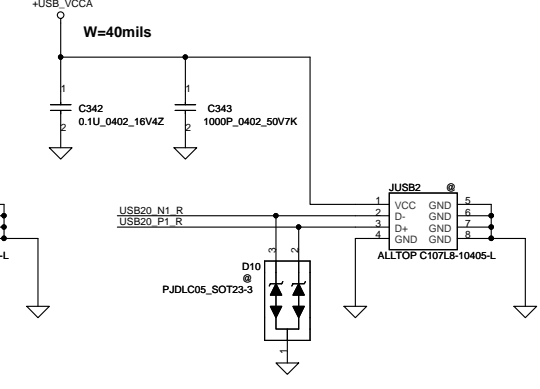
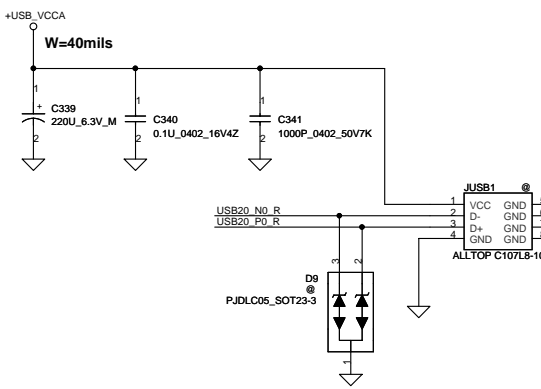
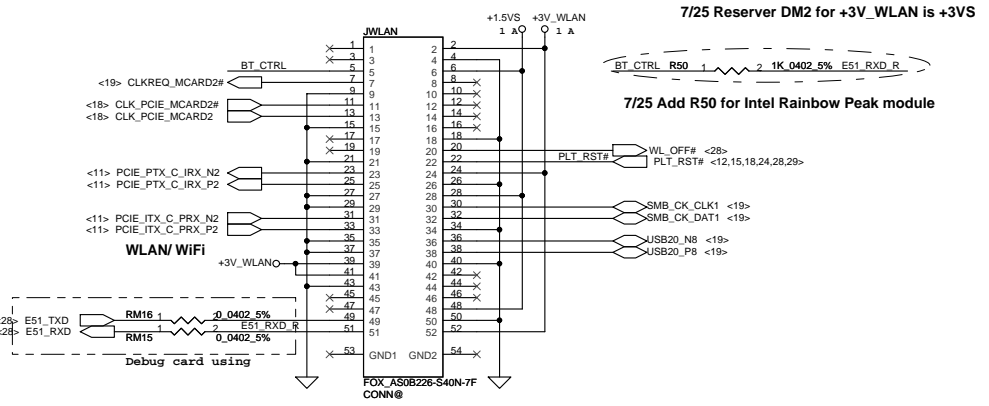
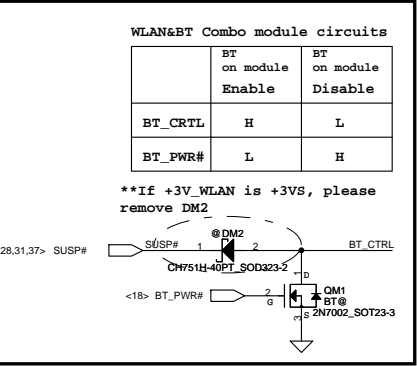
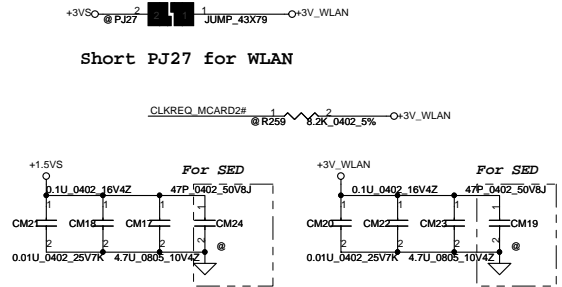
### SATA ODD Conn



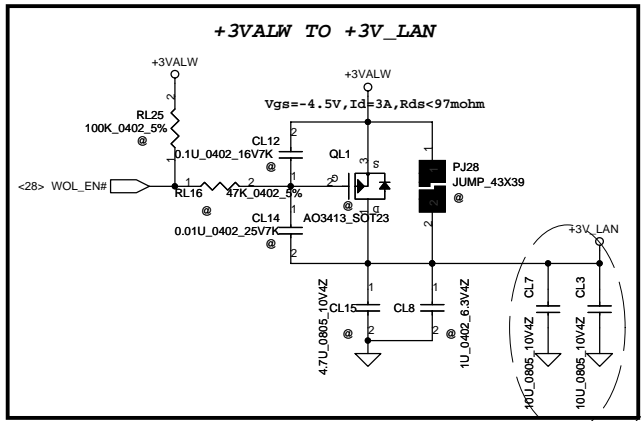
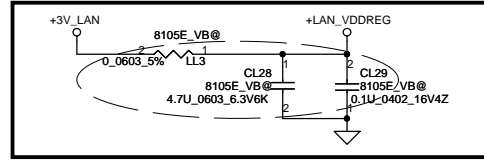
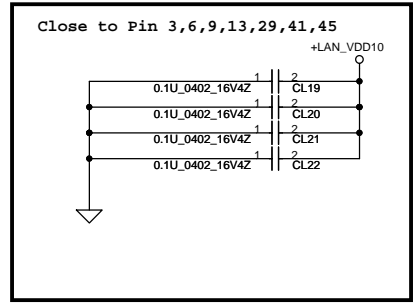
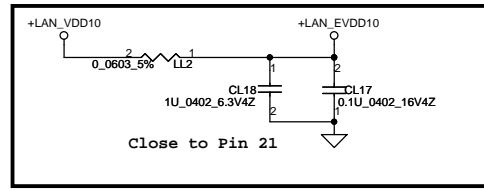
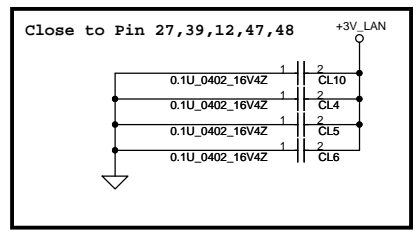
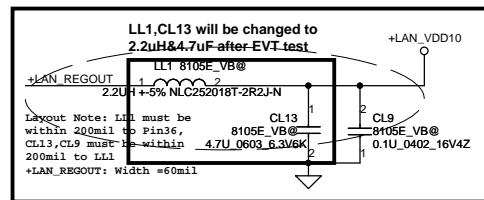
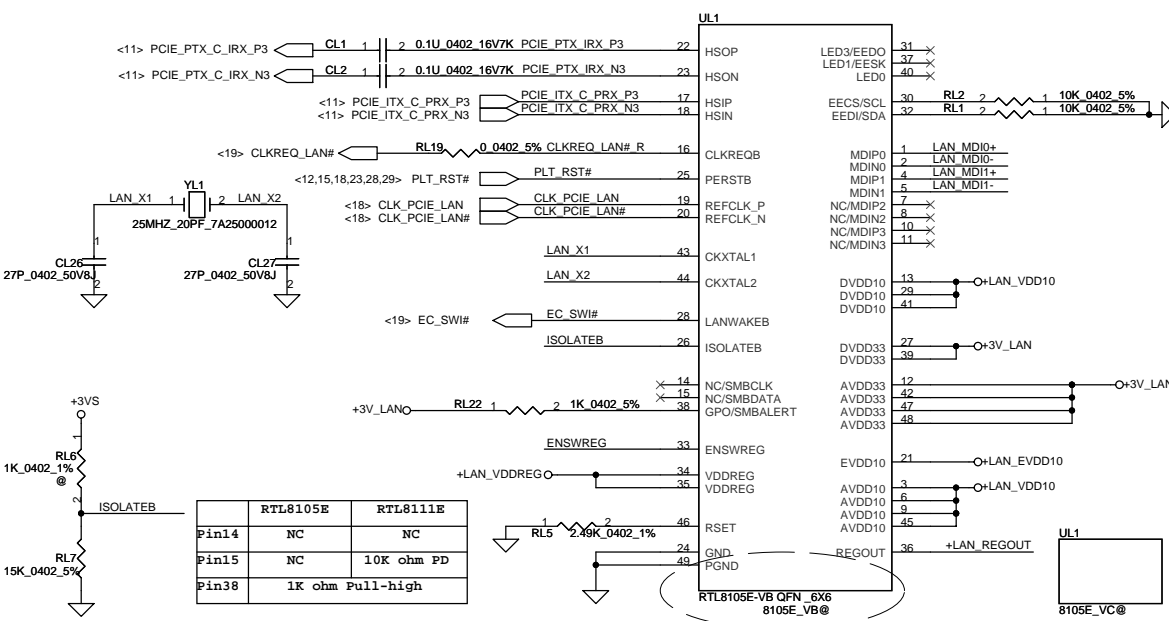
### USB Port 0 & Port1



### Slot#1 Half PCIe Mini Card-WLAN

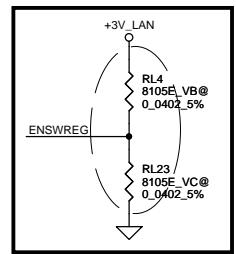


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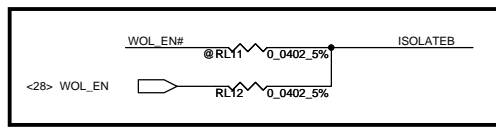


7/16 Change UL1 from RTL8105E-VB (SA00003PO10) to RTL8105E-VC (SA00003PO20)

7/16 For LDO mode :  
 1. Remove RL4, mount RL23.  
 2. Remove LL1, CL13, CL9, LL3, CL28, CL29.

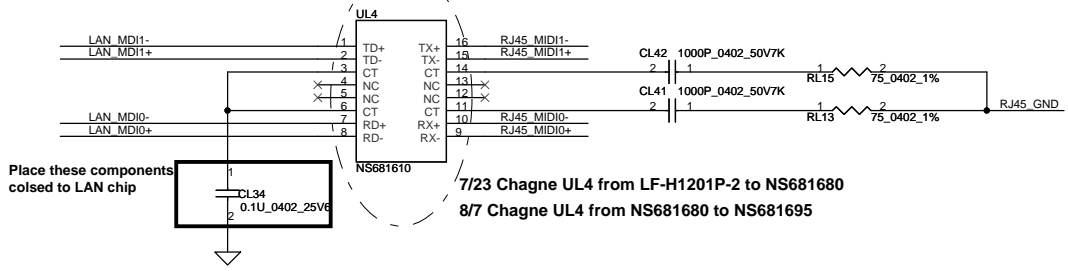
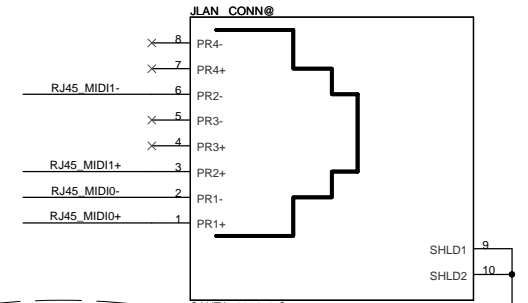


8/7 Chagne UL4 from NS681680 to NS681695

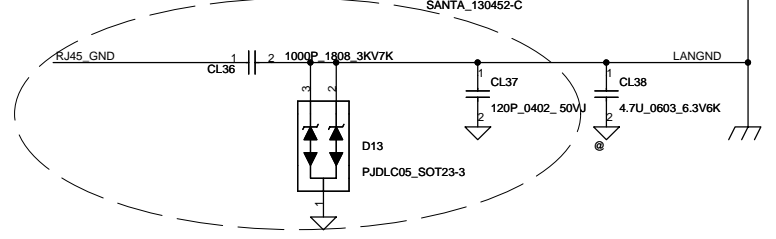


LAN Conn.

change connector to w/o LED  
 (use NPVAA LAN conn. before LAN symol ready)

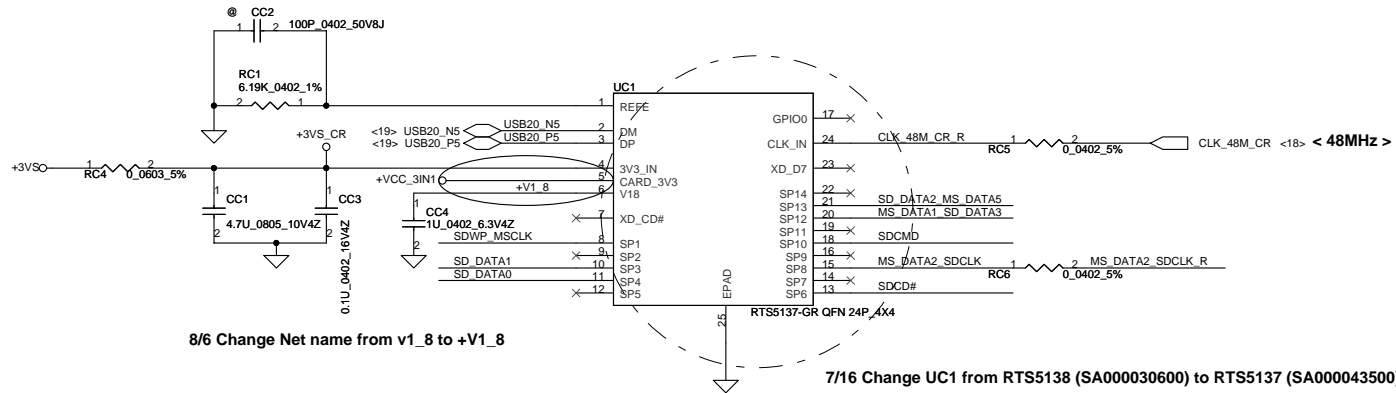


7/23 Chagne UL4 from LF-H1201P-2 to NS681680  
 8/7 Chagne UL4 from NS681680 to NS681695

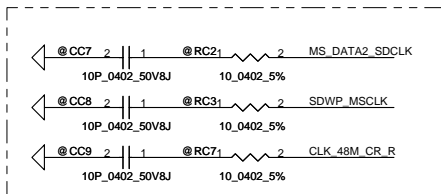


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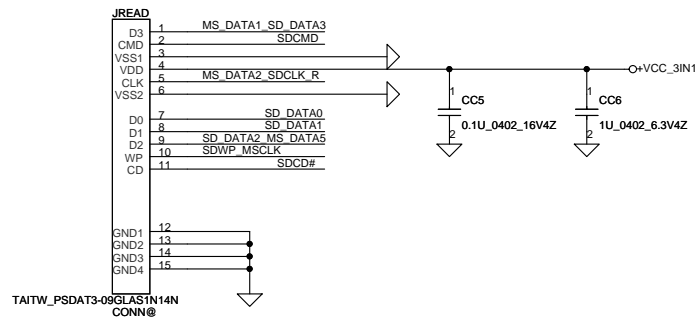




for EMI request

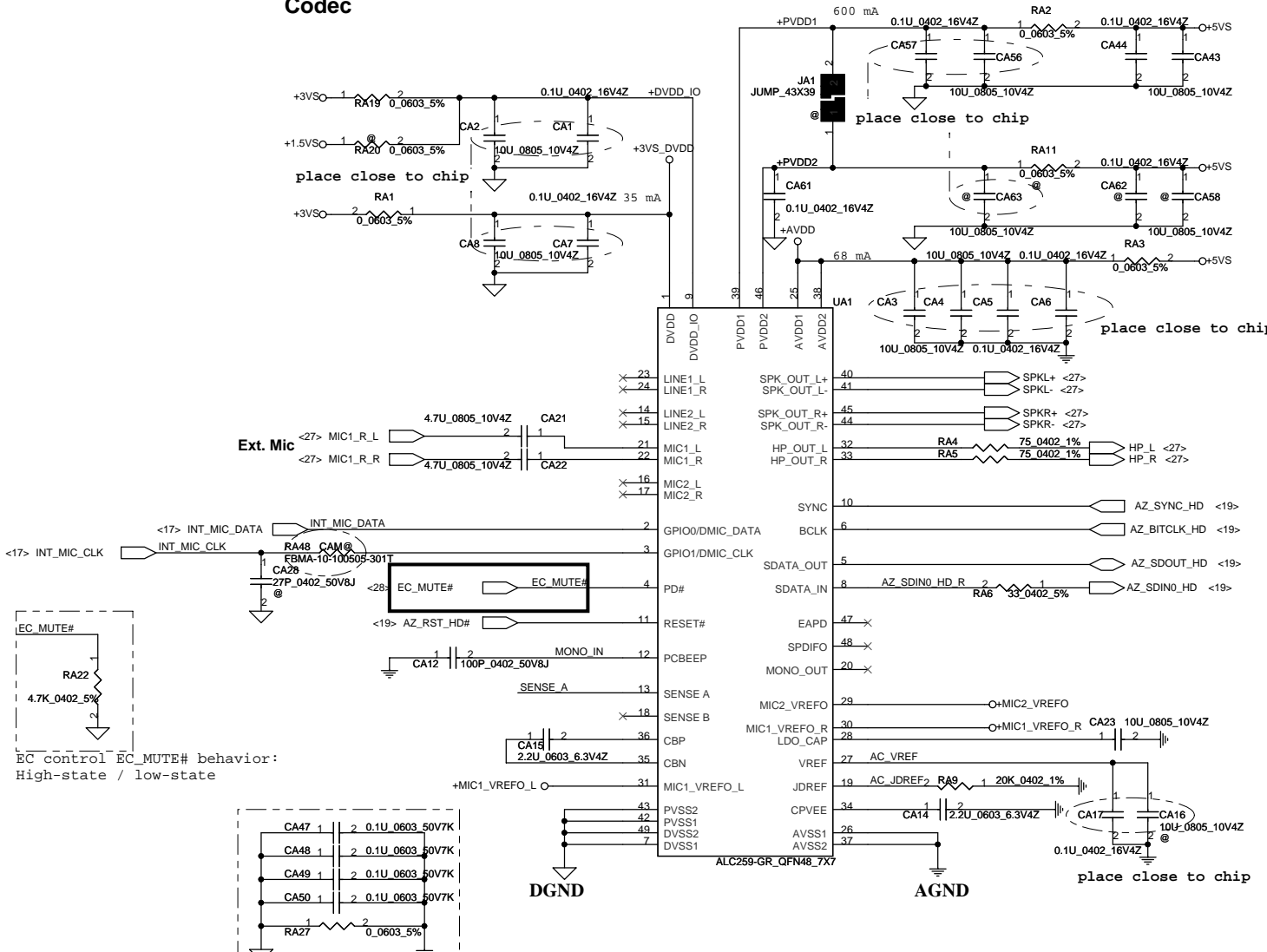


< 2 in 1 Card Reader >



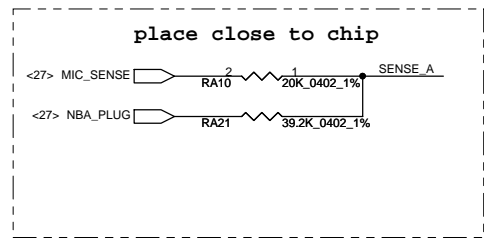
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# Codec

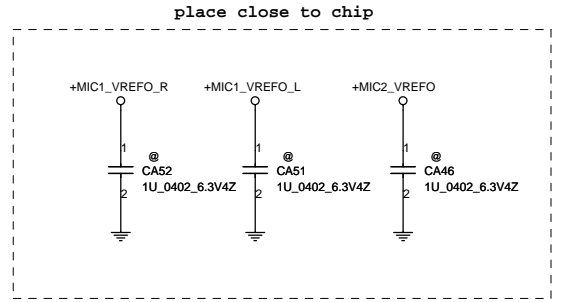
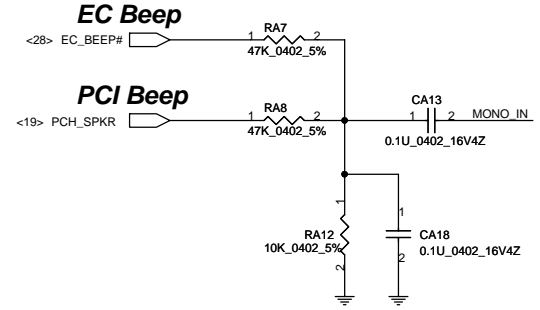


EC control EC\_MUTE# behavior:  
High-state / low-state

Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

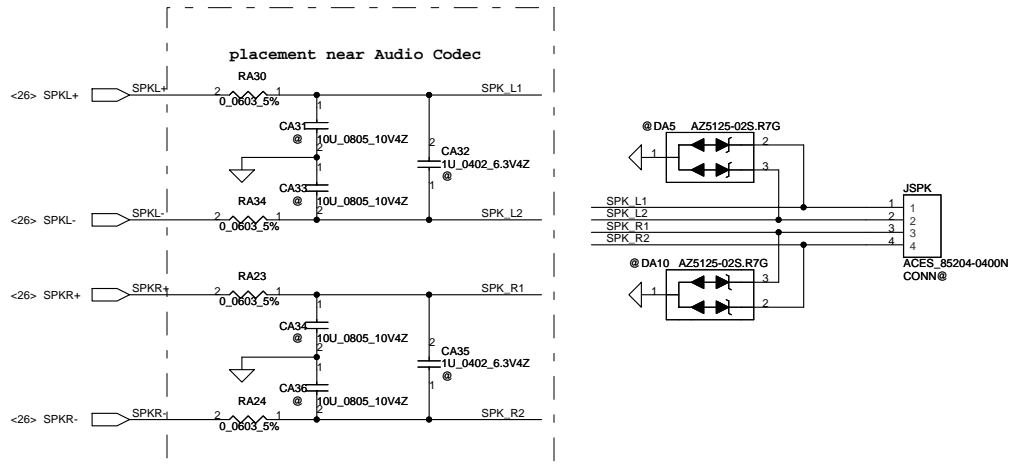


## Beep sound

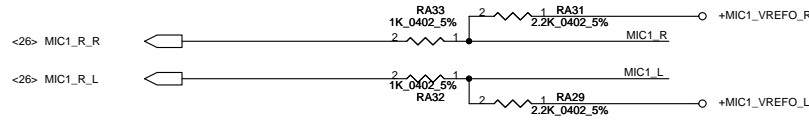


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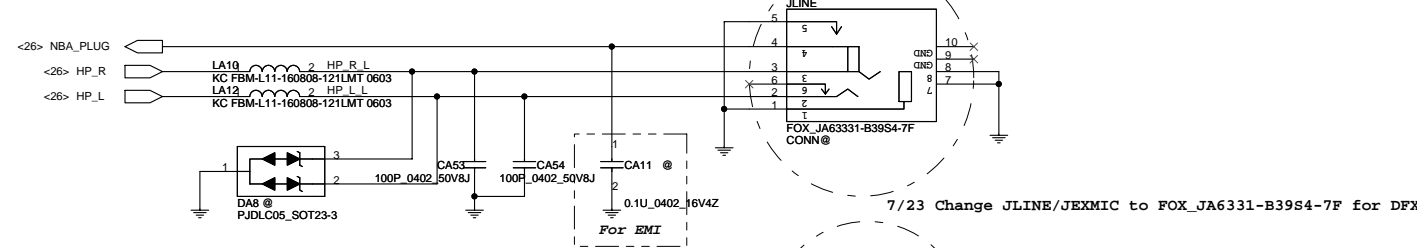
# Speaker Connector



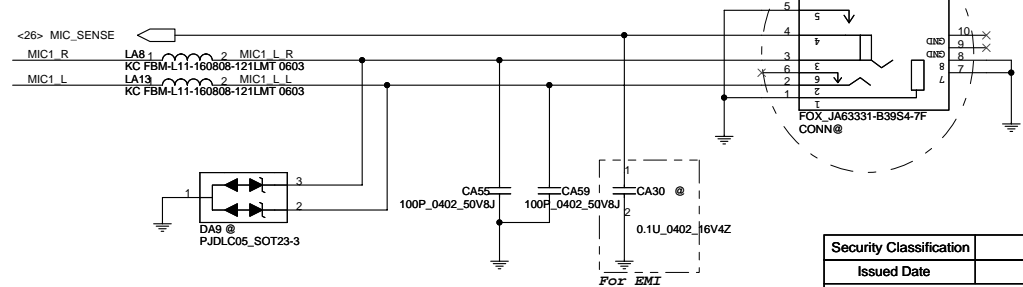
# Ext.MIC/LINE IN JACK



# HeadPhone/LINE Out JACK



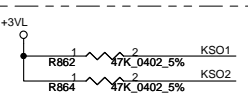
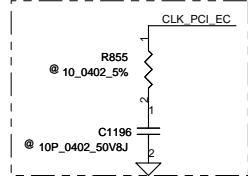
# Ext.MIC/LINE IN JACK



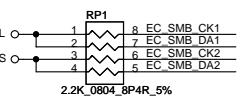
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**Compal Electronics, Inc.**  
**SCHEMATICS, MB A6843**

for EMI request

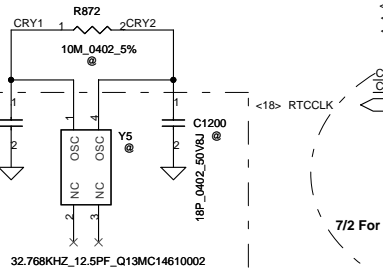


to avoid EC entry ENE test mode

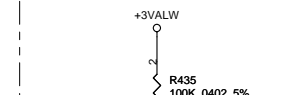
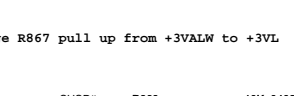
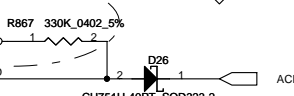
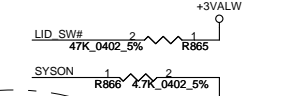
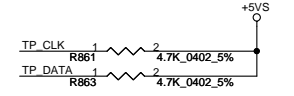
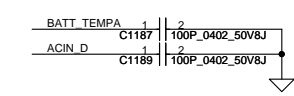
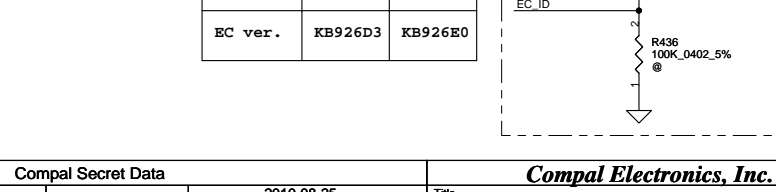
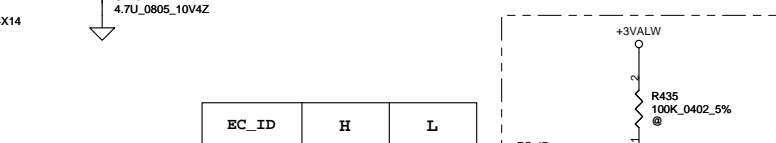
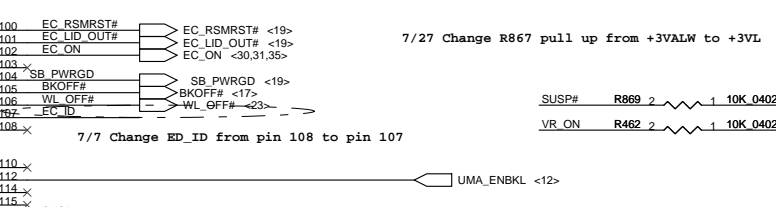
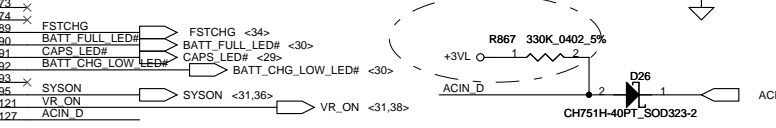
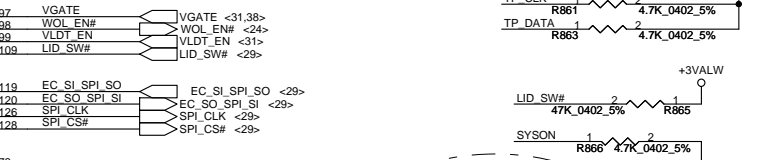
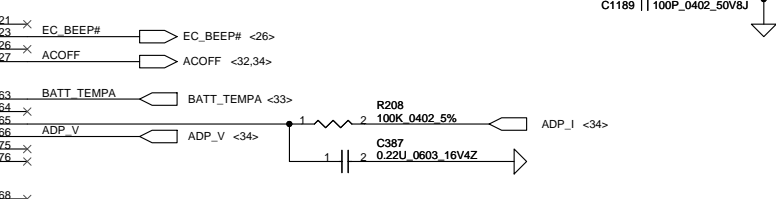
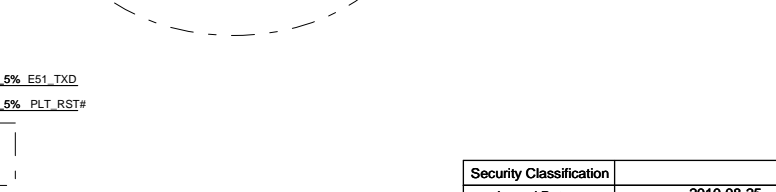
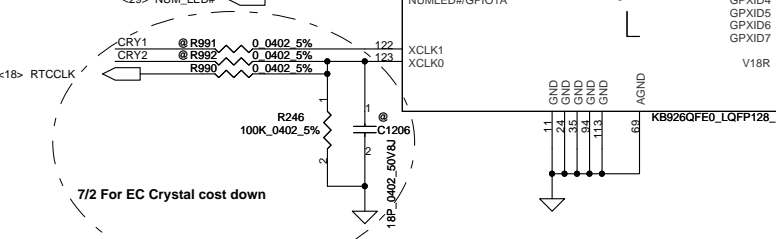
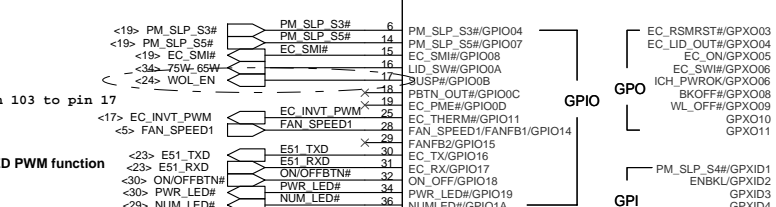
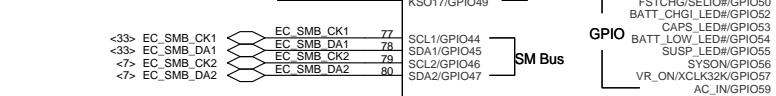
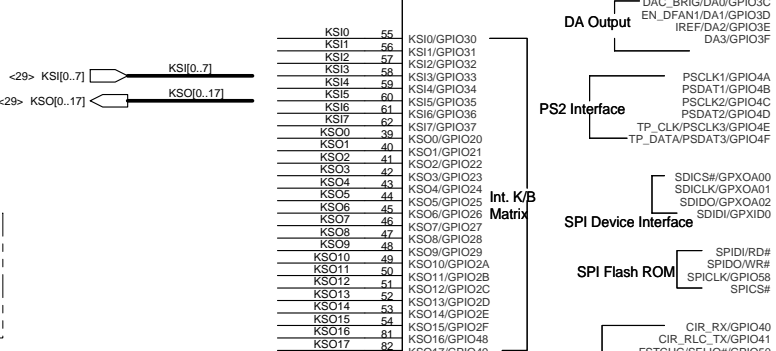
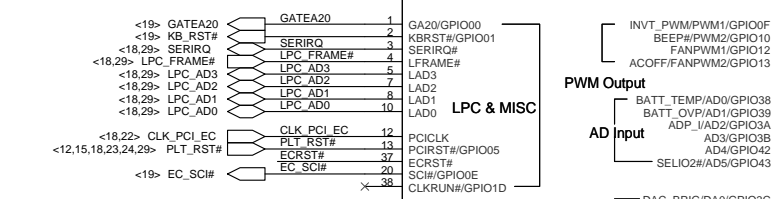
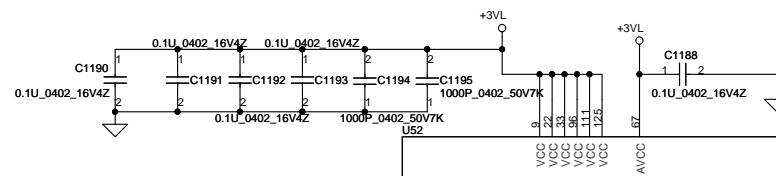
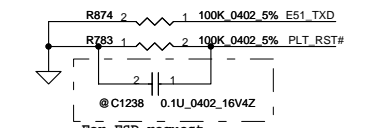


7/7 Change WOL\_EN from pin 103 to pin 17

7/6 For Power LED PWM function

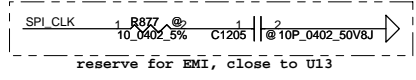
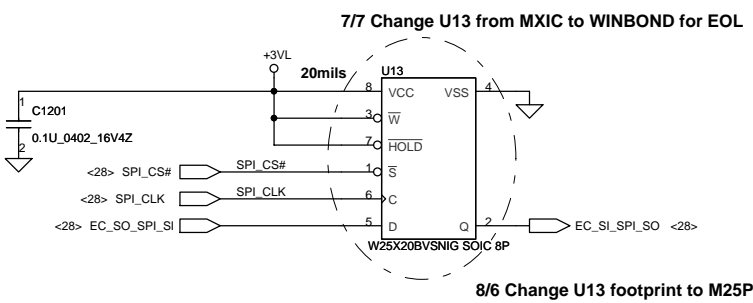


7/20 PVT reserve C1199, Y5, C1200

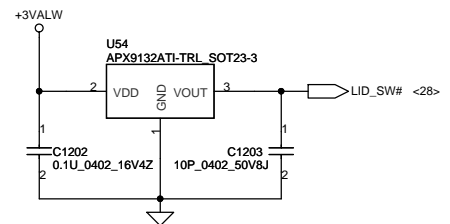


EC_ID	H	L
EC ver.	KB926D3	KB926E0

# SPI Flash (256KB)

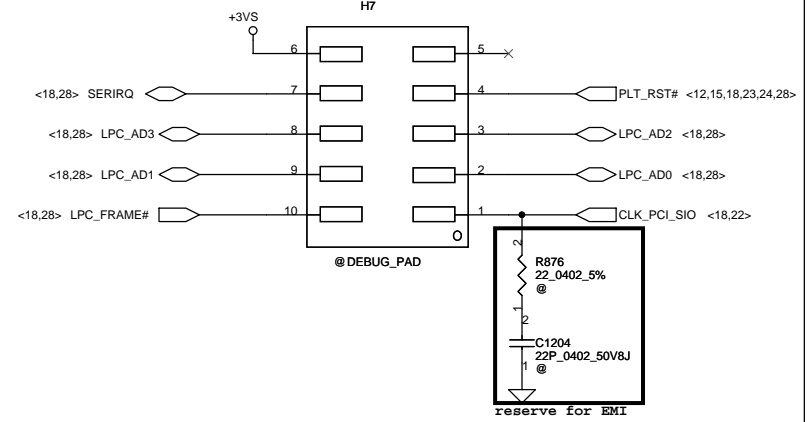


# Lid SW

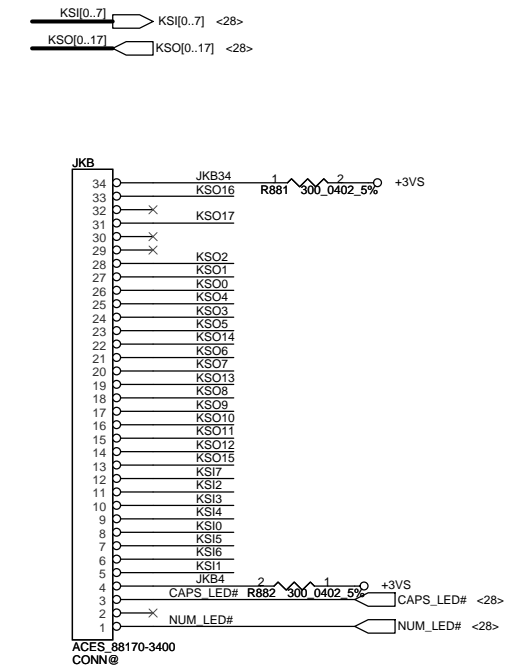


# LPC Debug Port

Please place the PAD under DDR DIMM.



# KEYBOARD CONN.

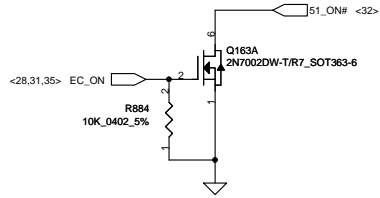
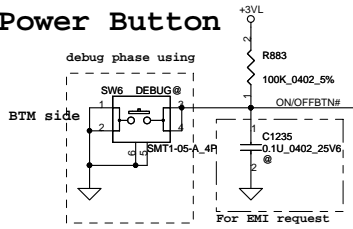


please close to JKB1

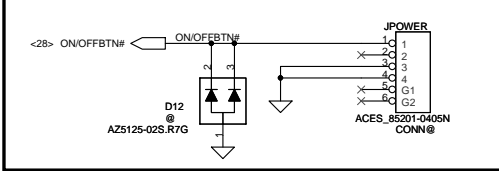
KSO16	1	2	100P_0402_50V8J
KSO17	1	2	100P_0402_50V8J
KSO2	1	2	100P_0402_50V8J
KSO1	1	2	100P_0402_50V8J
KSO0	1	2	100P_0402_50V8J
KSO4	1	2	100P_0402_50V8J
KSO3	1	2	100P_0402_50V8J
KSO5	1	2	100P_0402_50V8J
KSO14	1	2	100P_0402_50V8J
KSO6	1	2	100P_0402_50V8J
KSO7	1	2	100P_0402_50V8J
KSO13	1	2	100P_0402_50V8J
KSO8	1	2	100P_0402_50V8J
KSO9	1	2	100P_0402_50V8J
KSO10	1	2	100P_0402_50V8J
KSO11	1	2	100P_0402_50V8J
KSO12	1	2	100P_0402_50V8J
KSO15	1	2	100P_0402_50V8J
KSI7	1	2	100P_0402_50V8J
KSI2	1	2	100P_0402_50V8J
KSI3	1	2	100P_0402_50V8J
KSI4	1	2	100P_0402_50V8J
KSI0	1	2	100P_0402_50V8J
KSI5	1	2	100P_0402_50V8J
KSI6	1	2	100P_0402_50V8J
KSI1	1	2	100P_0402_50V8J
CAPS_LED#	1	2	100P_0402_50V8J
NUM_LED#	1	2	100P_0402_50V8J

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### Power Button

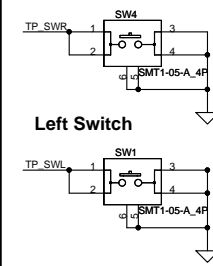


### < Power / B Connector >

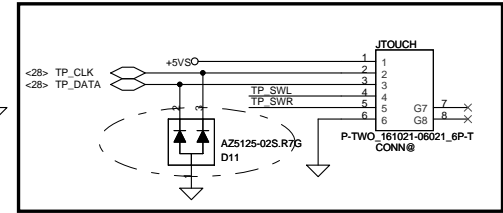
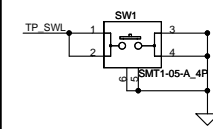


### < Touch / B Connector >

#### Right Switch



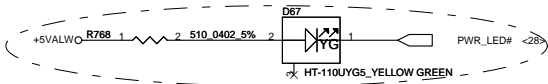
#### Left Switch



7/13 For ESD request

### POWER/SUSPEND LED

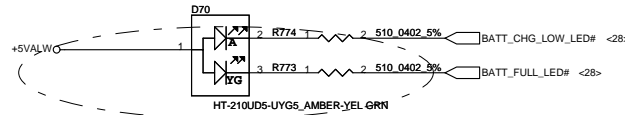
Vf=1.9V(typ), 2.4V(max)  
If=20mA(max)



- 7/6 For Power LED PWM function
- 7/15 Change D67/D70 to 5mA type
- 7/23 Change R773 from 120 to 510 ohm
- 7/23 Change Net name from +3VALW to +5VALW

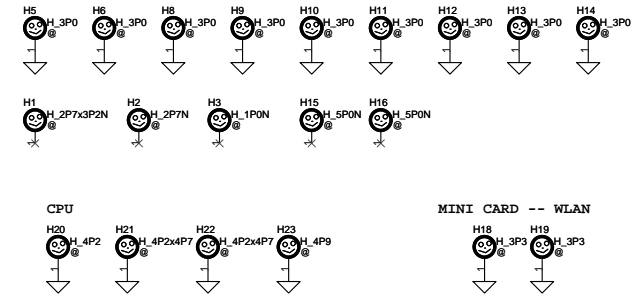
### DC IN/ BATT CHARGE

Vf=1.8V(typ), 2.0V(max) for amber  
Vf=1.8V(typ), 2.0V(max) for green  
If=20mA(max)

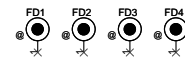


- 7/23 Change R773 from 120 to 510 ohm
- 7/23 Change Net name from +3VALW to +5VALW
- 8/6 Add R774 link to BATT\_CHG\_LOW\_LED#
- 8/6 Change R773 link to BATT\_FULL\_LED#

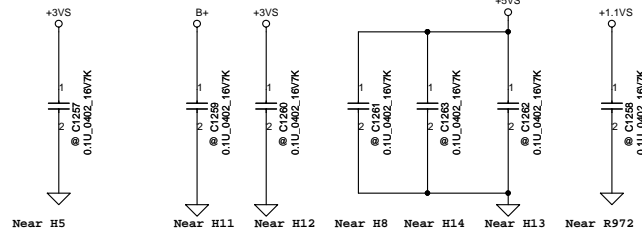
### Screw Hole



### PCB Fedical Mark PAD

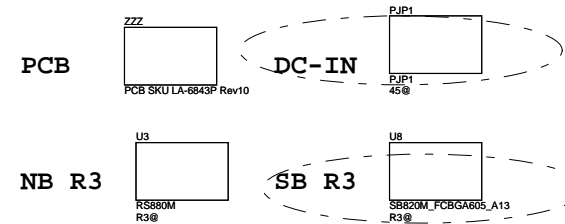


### ESD reserved



### ISPD

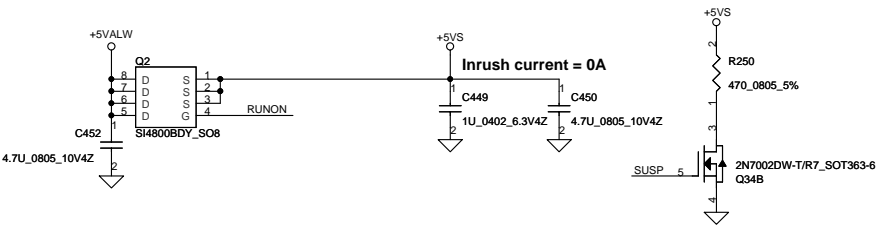
7/13 Change P/N to DC30100A400



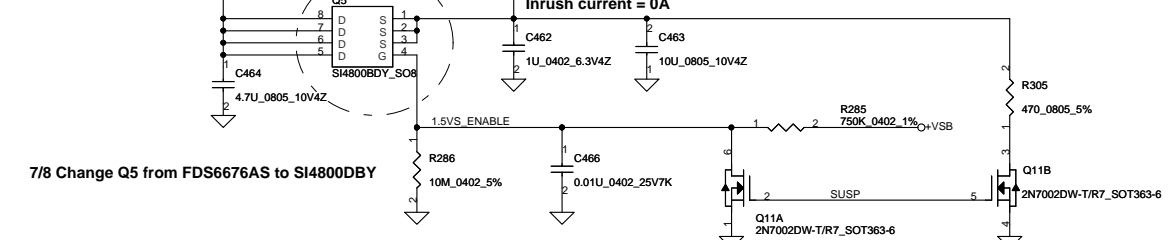
7/21 Change P/N to SA00031WB0

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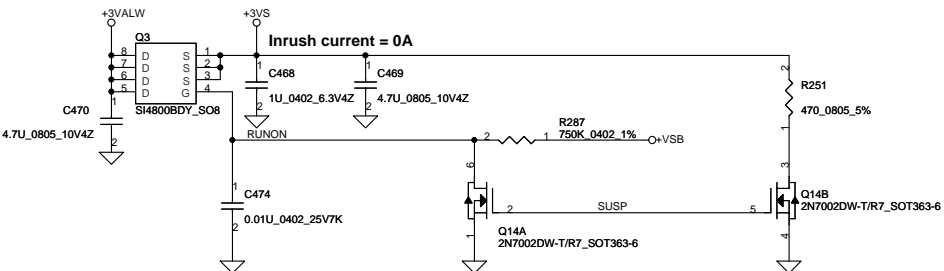
< +5VALW TO +5VS >



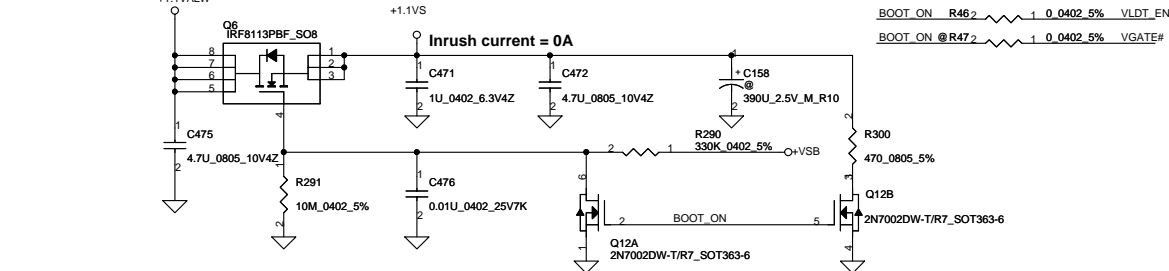
< +1.5V TO +1.5VS >



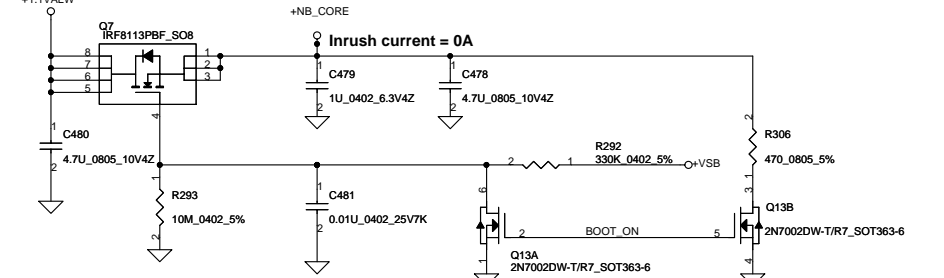
< +3VALW TO +3VS >



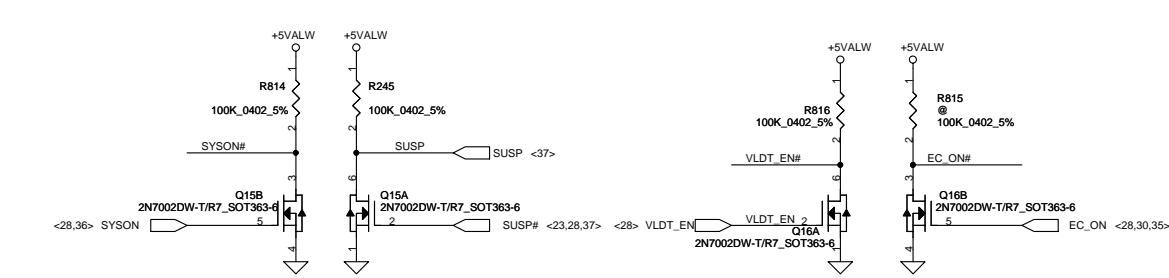
< +1.1VALW TO +1.1VS >



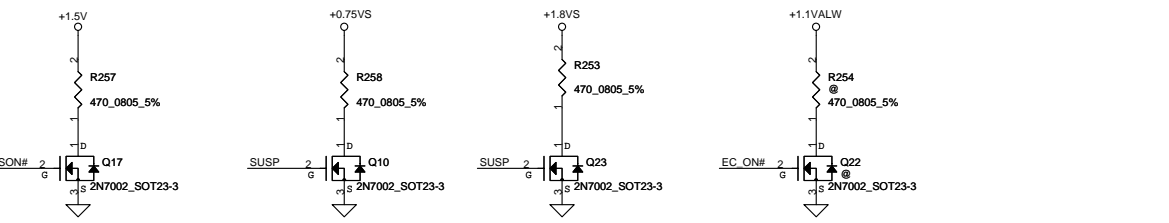
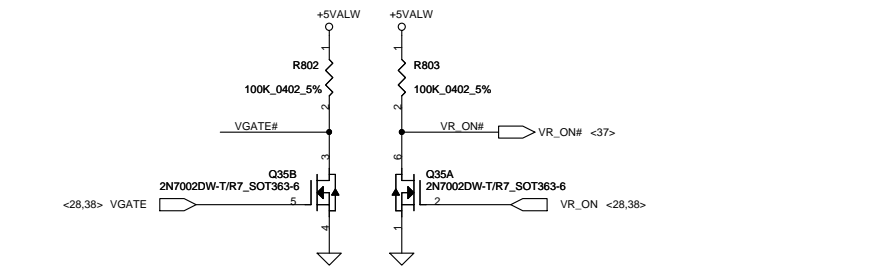
< +1.1VALW TO +NB\_CORE >



< Inversion of SYSON, SUSP#, VLDT\_EN, EC\_ON >



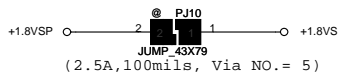
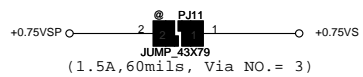
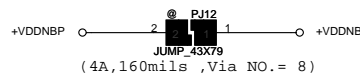
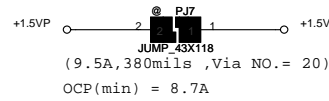
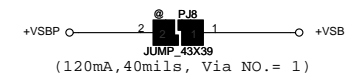
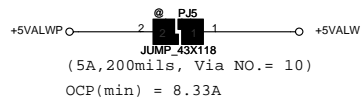
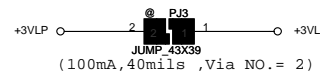
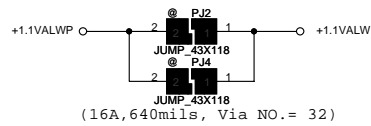
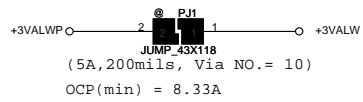
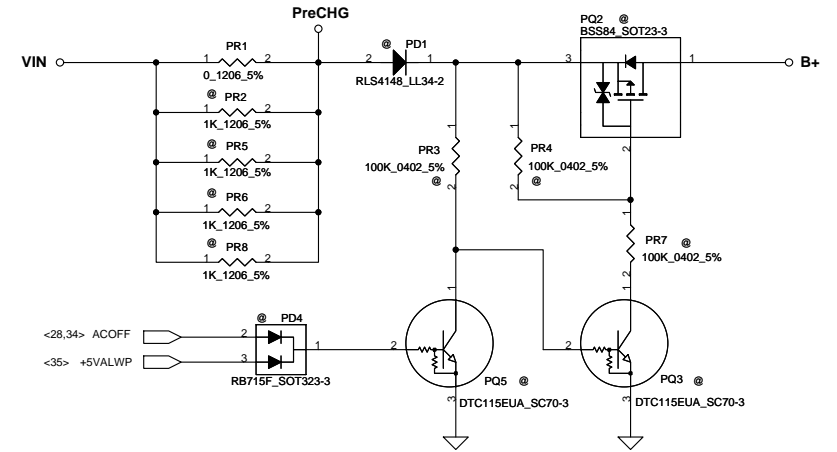
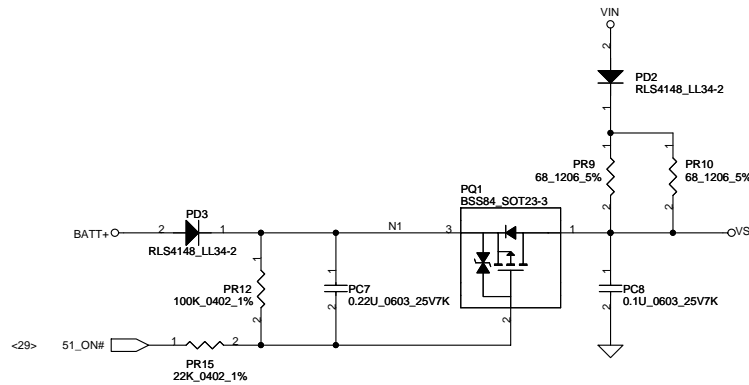
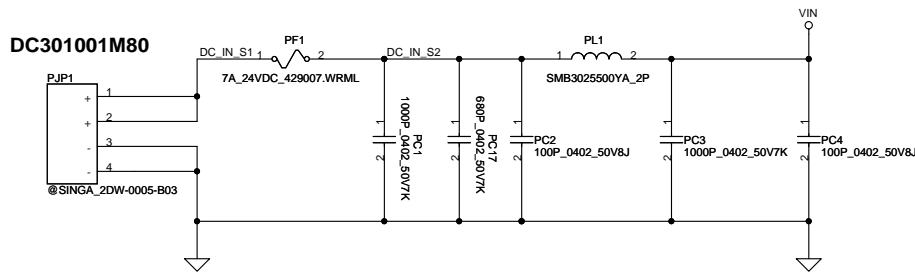
< Discharge circuit >



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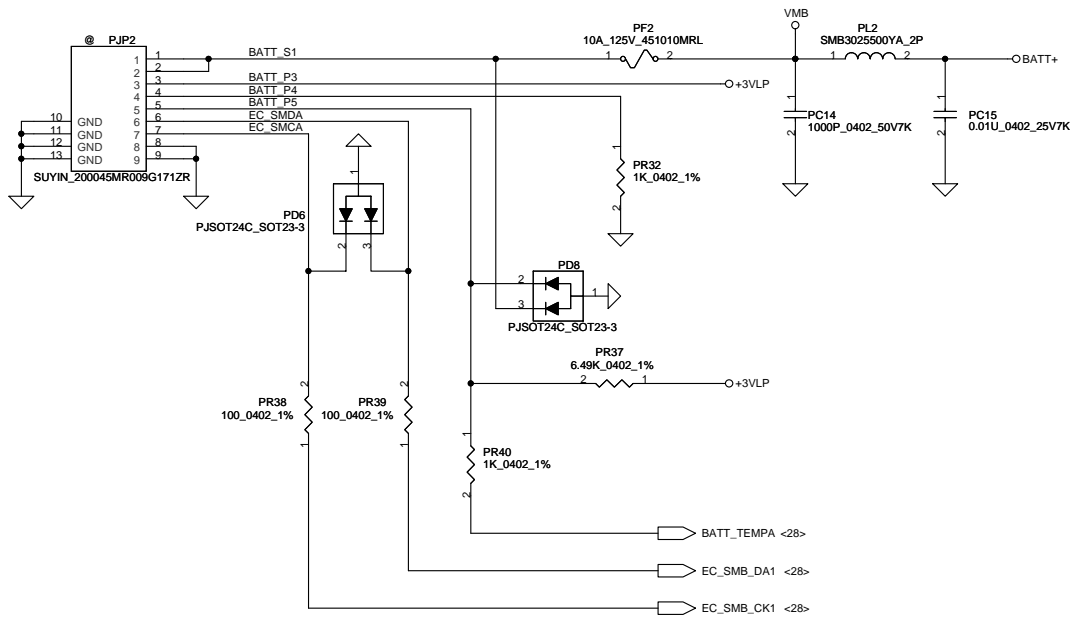
**DC301001M80**



**Precharge detector  
15.97V/14.84V FOR  
ADAPTOR**

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PH1 under CPU botten side :  
 CPU thermal protection at 95 degree C  
 Recovery at 56 degree C

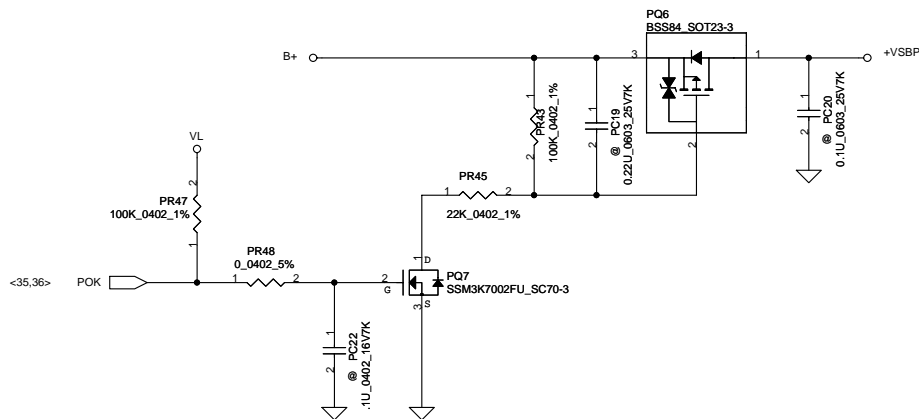
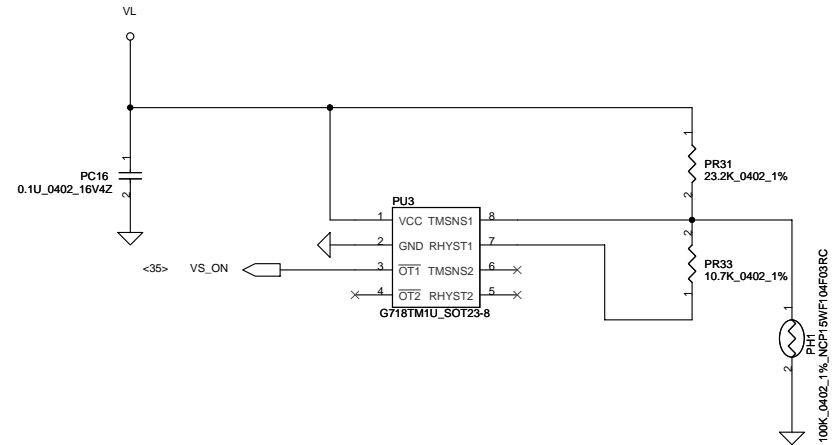
$$R_{set} = 3 * R_{tmh}$$

$$R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$$

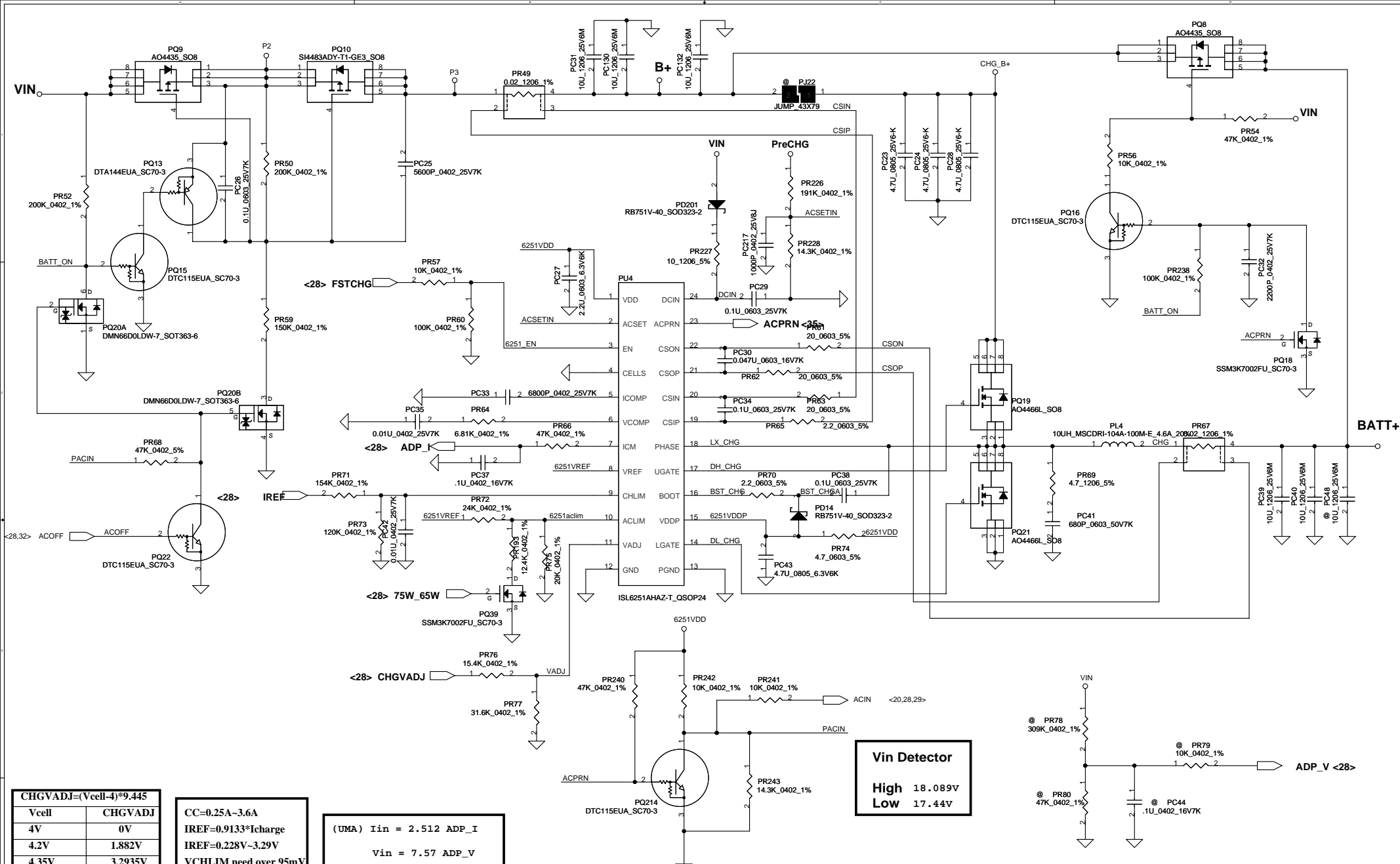
$$R_{tmh} \text{ at } 95C = 6.64K, R_{tml} \text{ at } 57C = 25.1K$$

$$R_{set} = 3 * 6.64K = 19.92K \Rightarrow 20K$$

$$R_{hyst} = (20K * 25.1K) / (3 * 25.1K - 20K) = 9.078K \Rightarrow 9.09K$$



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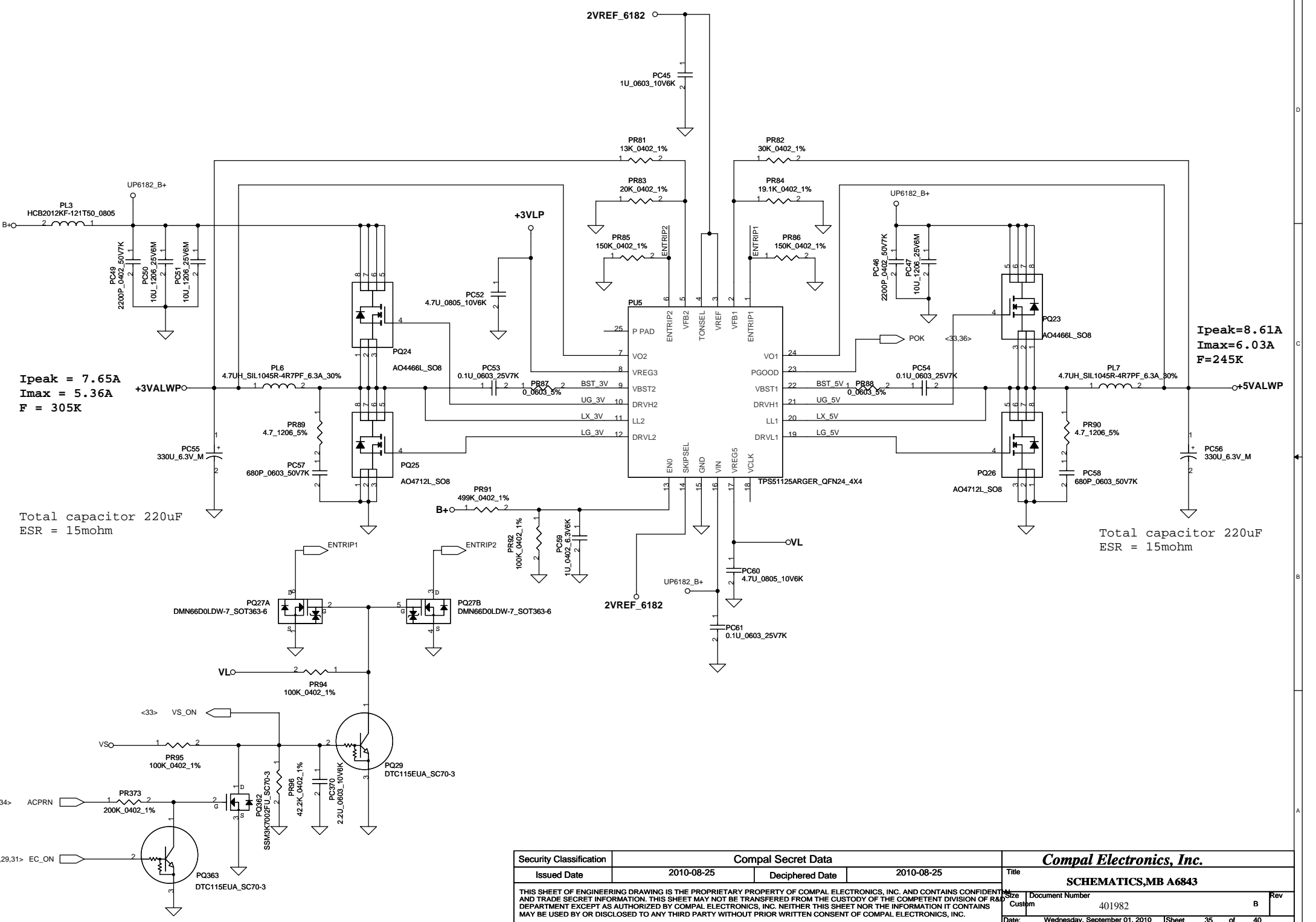
**Vin Detector**  
 High 18.089V  
 Low 17.44V

<b>CHGVADJ=(Vcell-4)*9.445</b>	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

**CC=0.25A-3.6A**  
**IREF=0.9133\*Icharge**  
**IREF=0.228V-3.29V**  
**VCHLIM need over 95mV**

**(UMA) Iin = 2.512 ADP\_I**  
**Vin = 7.57 ADP\_V**

UMA Iada=0-3.421A (65W) CP=3.15A PR49=0.02, PR72=24k, PR75=20k, PR35=11.5K, 75W\_65W=high  
 Iada=0-3.947A (75W) CP=3.63A PR49=0.02, PR72=24k, PR75=20k, PR35=11.5K, 75W\_65W=low  
 CP= 92%\*Iada



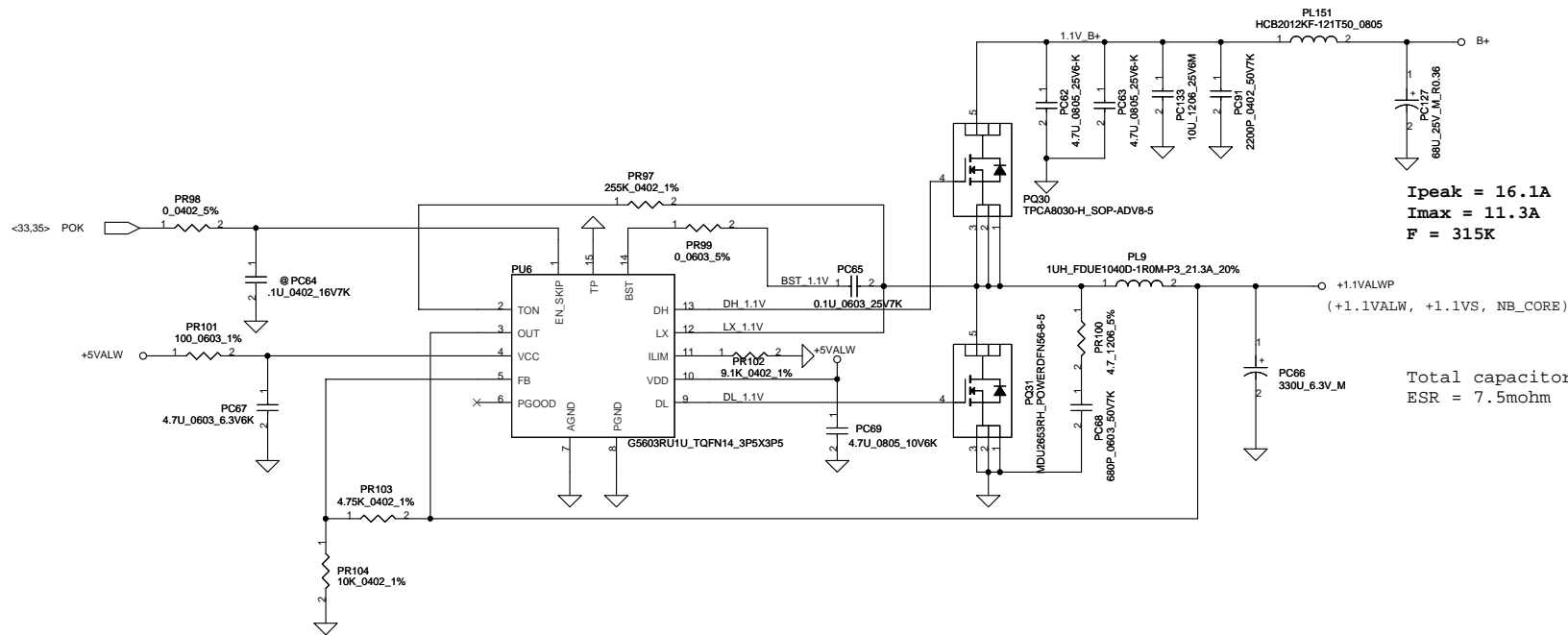
I<sub>peak</sub> = 7.65A  
 I<sub>max</sub> = 5.36A  
 F = 305K

Total capacitor 220uF  
 ESR = 15mohm

I<sub>peak</sub> = 8.61A  
 I<sub>max</sub> = 6.03A  
 F = 245K

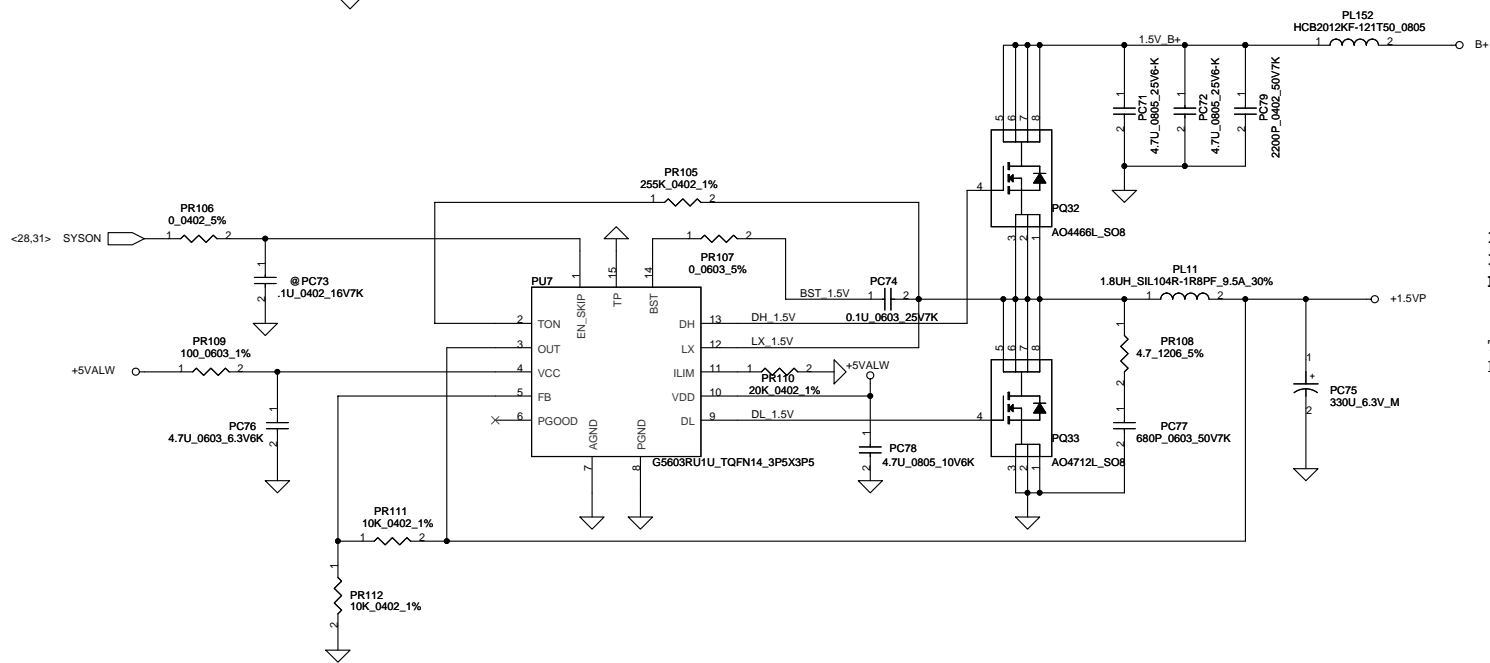
Total capacitor 220uF  
 ESR = 15mohm

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$I_{peak} = 16.1A$   
 $I_{max} = 11.3A$   
 $F = 315K$

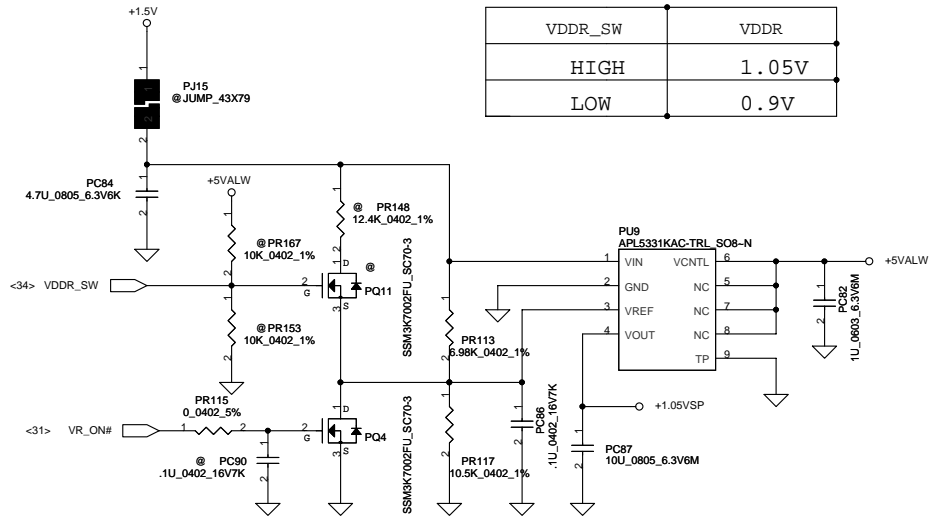
Total capacitor 550uF  
 ESR = 7.5mohm



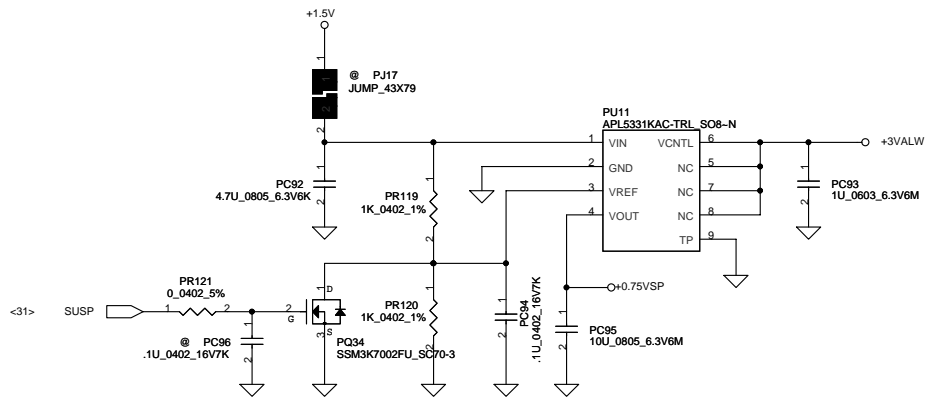
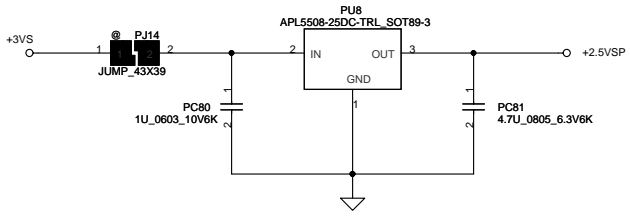
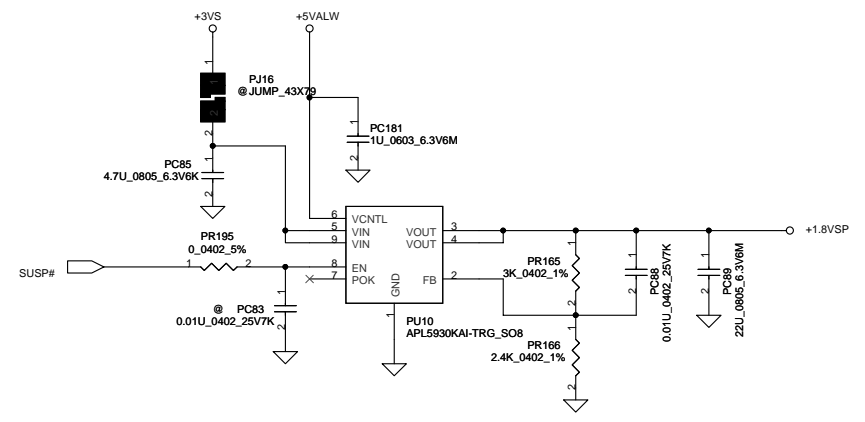
$I_{peak} = 9.5A$   
 $I_{max} = 6.65A$   
 $F = 315K$

Total capacitor 220uF  
 ESR = 15mohm

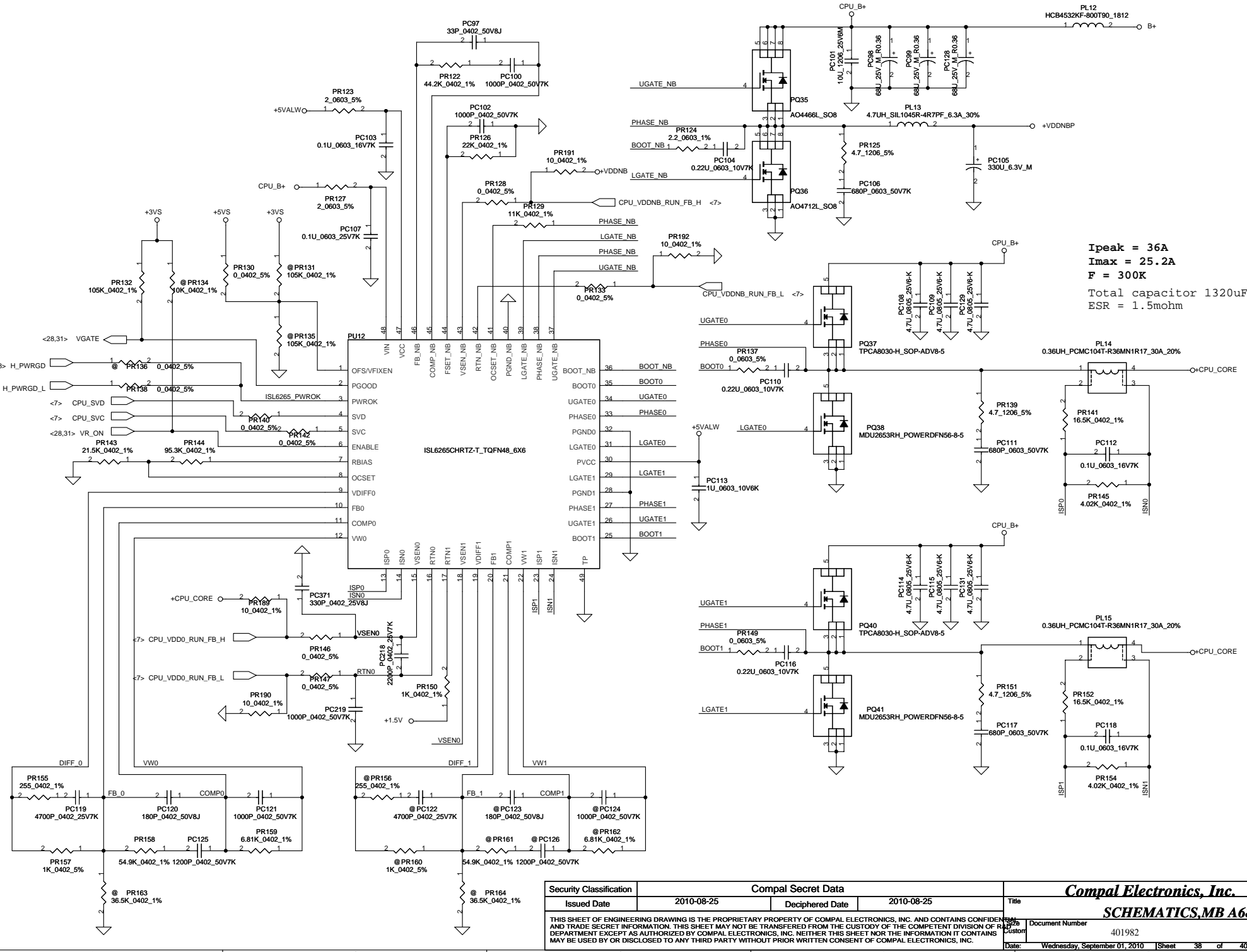
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VDDR_SW	VDDR
HIGH	1.05V
LOW	0.9V



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**I<sub>peak</sub> = 36A**  
**I<sub>max</sub> = 25.2A**  
**F = 300K**  
 Total capacitor 1320uF  
 ESR = 1.5mohm

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# PIR (Product Improve Record)

PWAE LA-6843P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2010/07/20	28	Reserve CL199,Y5,C1200	For design change
2	2010/07/20	28	Reserve R436 for only KB926E0	For design change
	2010/07/20	29	Del R875	For SERIRQ direct connect to H7.7
	2010/07/20	29	Del C888/C889/Y4/R368	For design change
3	2010/07/21	11-15	Change US R1 P/N from A12(SA000032WT40) to A13(SA000032WA0)	For SB820 A13 version
	2010/07/21	30	Change US R3 P/N from A12(SA000032WI50) to A13(SA000032WB0)	For SB820 A13 version
4	2010/07/23	18	Change D8 from DAN202U to CHN202UPT	For design change
5	2010/07/23	24	Change U4 from LF-HL201P-2 to LFE8456E-R for use 5mA type	For design change
6	2010/07/23	30	Change R768/R773 from 120 to 510 ohm for use 5mA type	For design change
	2010/07/23	30	Change R768.1 pull up from +3VALW to +5VALW for use 5mA type	For design change
7	2010/07/23	27	Change JLINE/JEXMIC to FOX_JA6331-B3984-7F	For DFX request
8	2010/07/26	23	Reserve DM2	For +3V_MLAN is +3VS
9	2010/07/26	24	Add R50	For Intel Rainbow Peak module
	2010/07/26	24	Reserve CL39	For EMI request
10	2010/07/27	28	Change R867 pull up from +3VALW to +3VL	For design change

REVISION CHANGE: 0.2 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2010/08/06	29	Change U13 footprint to M25P10-AVNM6T-SOP	For design change
2	2010/08/06	25	Change Net name form V1.8 to +V1.8	For customer request
	2010/08/06	29	Add R774 link to BATT_CHG_LOW_LED#	For customer request
	2010/08/06	29	Change R773 link to BATT_FULL_LED#	For customer request
3	2010/08/06	30	Reserve SW6 Del SWS	For debug phase
	2010/08/09	30	Change U4 from NS681680 to NS681610	For design change
4	2010/08/09	08	Mount C26/C89,Reserve C24,C90	For design change
5	2010/08/16	18	Del R42/C94	For EMI request
	2010/08/16	18	Reserve CC9/RC7	For EMI request
6	2010/08/16	24	Add CL3/CL7 link to +3V_LAN	For EMI request
	2010/08/16	24	Reserve CL38	For EMI request
	2010/08/16	24	Change CL37 from 0.1uF to 120 pF	For EMI request
	2010/08/16	24	Add D13 link to LANGND	For EMI request

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# Version Change List ( P. I. R. List ) for Power Circuit

NO DATE	PAGE	MODIFICATION LIST	PURPOSE	Rev.
<i>2010 . 06 . 21 Release</i>				
<i>2010 . 07.25 modification list</i>				
	P 33	PC16 change to SE070104Z80	Defore material EOL	PVT
	P 38	PU12 change to SA000022M80	Before material MP schedule will impact PWWAE MP schedule	PVT
	P 33	Remove PD6 , PD8 @	ESD test fail	PVT
	P 34	Add PC132 , remove PC130 , PC131 , PR69 , PC41 @	For EMI fail	PVT
	P 35	Add PC51 , remove PC49 , PC46 , PC57 , PC58 , PR89 , PR90 @	For EMI fail	PVT
	P 36	Add PC79 , PC91 , PC133 , remove PR100 , PR108 , PC68 , PC77 @	For EMI fail	PVT
	P 38	Remove PR125 , PR139 , PR151 , PC106 , PC111 , PC117 @	For EMI fail	PVT
<i>2010 . 08.10 modification list</i>				
	P 37	Change PU9 , PU11 to SA053310110	UP7711 stop using from now on	Pre-MP
	P 38	Add PC218 , PC219 , PC371	For VCORE Ripple	Pre-MP
	P 32	Add PR8	For Precharge rising current	Pre-MP
	P 32 , P 33	PQ1 , PQ2 , PQ6 change to SB900840003	SB906100210 material delivery had problem	Pre-MP
<i>2010 . 08.16 modification list</i>				
	P 35	Change PU5 to SA000020C80	UPI product stop using	Pre-MP
<i>2010 . 08.17 modification list</i>				
	P 34	Change PU4 to SA00001EP80	SA00003TK00 stop using	Pre-MP
	P 38	Remove PR127 @	To solve +1.1VALW noise	Pre-MP
<i>2010 . 08.23 modification list</i>				
	P 34	Remove PR193 , PQ39 @	For PWWAE MP use 25W CPU	Pre-MP

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